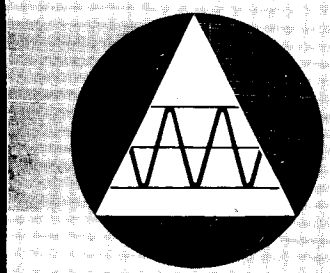

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INHIBIT - CORE LOGIC STUDY
FINAL REPORT

February 1963

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CONTENTS

CONTENTS (Continued)

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

TABLES

NOMENCLATURE

Term	Symbol	Description
Register Memory		Core memory wound to provide bit-time to bit-time storage. Includes all register cores.
Logic Memory		Core memory inhibit wound to perform logic. Includes all logic cores.
Logic Module		One plane of the logic memory. Contains one or more logic matrices.
Logic Matrix		A group of cores wound as a particular logic function and therefore linked by a common sense line.
Logic Read Clock	C_{LR}	Current pulse used to read and reset logic matrices.
Register Read Clock	C_{RR}	Current pulse used to read and reset register cores
Logic Write Clock	C_{LW}	Current pulse used to strobe the logic inhibit terms and set the logic matrices.
Register Write Clock	C_{RW}	Current pulse used to strobe the register inhibit terms and set the logic matrices.
System Clock	C	Logical summation of the four read and write clocks which occur in the order: Register Read, Logic Write, Logic Read, and Register Write.
Bit Time	P_i	Single system clock cycle starting and ending at the beginning of the register read clock pulse.
Pulse Time$_{i(x)}$ Clock	$PC_{i(x)}$	Current pulse occurring during the i^{th} bit time coincident with the x^{th} part of that bit cycle (x = logic read, register read, logic write, or register write)

NOMENCLATURE (Continued)

Term	Symbol	Description
Inhibit Pulse	I_i	Current pulse generated by a flip-flop output used as a logic signal to inhibit the setting of logic or register cores.
Logic Memory "One" Output Pulse	V_{1L}	Signal appearing on a logic matrix sense line at logic read time when the matrix had been previously set to the "one" state.
Logic Memory "Zero" Output Pulse	V_{0L}	Signal appearing on a logic matrix sense line at logic read time when the matrix had previously been in the "zero" state.
Register Memory "One" Output Pulse	V_{1R}	Signal appearing on a register sense line at register read time when the register core interrogated had previously been in the "one" state.
Register Memory "Zero" Output Pulse	V_{0R}	Signal appearing on a register sense line at register read time when the register core interrogated had previously been in the "zero" state.
Flip-Flop		Register/Logic memory time shared sense amplifier plus quarter bit delay. Also called transfer circuit.
Active Lines		Includes all lines within the logic memory required by the logic which may carry pulsed current; i.e., all clock and inhibit lines.

1. INTRODUCTION

1.1 Purpose of Study

The purpose of the investigations conducted under the JPL Inhibit Core Logic Study Contract was to acquire information and make recommendations for the packaging, production process, and ferrite core buy-in specification for the logic memory to be used in the inhibit core logic computer specified by JPL. The specific tasks to be performed in each of these areas are presented below to provide some basis for evaluating the discussions presented later in the report.

1.1.1 Packaging and Production Processes

The major effort will be expended in this area. The study will be divided into four sections covering mechanical configuration, materials selection, production processes and final wire routing. The configuration study will be directed toward achieving a mechanically reliable package which is easy to manufacture and maintain. The materials study will attack the problem of material compatibility in the spacecraft environment. The manufacturing process study will attempt to optimize the procedure for assembling the materials into the final configuration in terms of quality assurance and cost. The overall output of the packaging task will be to provide JPL with a complete assembly process description, a set of drawings which detail the construction of the logic module, and a sound overall approach for assembling the modules into a final memory package. To facilitate the production process, means will be incorporated into the module structure for accommodating an in-process wiring verification method. As an adjunct to the manufacturing process, a study will be conducted on the feasibility of using an IBM 7090 computing system to produce the final wiring lists.

1.1.2 Ferrite Core Buy-in Specification

This effort will be directed toward providing JPL with a detailed test procedure and adequate quality control criteria to permit purchase of logic cores with the.

best possible assurance for provision of logic matrix characteristics which are reliable, repeatable and compatible with the rest of the system. A general matrix specification will also be determined which will provide JPL with adequate design information for an evaluation of JPL flip-flops and current drivers. The matrix specification will be generated only after an optimized matrix configuration has been devised. Optimization will be considered from both the mechanical and electrical system requirements.

1.1.3 Test Equipment

A final section will include paper designs of a production wiring verification tester and a logic memory system tester. The production tester will be designed to be incorporated into the production line so that it may be used whenever required without disrupting the process. It will be required to give 100 percent wiring verification automatically and rapidly and be compatible with the module configuration devised in the packaging study. The memory system tester, called the maintenance tester, will be designed for use in module and system buy-in and maintenance. Because of the limited number of systems contemplated, it will be presented as manually operated equipment. Its organization, however, will be such as to make it easily automated.

1.2 System Description

A brief description of the overall inhibit core logic system is presented in order to clarify the problems associated with the tasks to be performed under this contract. This system was first presented in an unpublished report by L. A. Andrews of the National Cash Register Company, entitled A Technique for Using Memory Cores as Logical Elements. The system described in this report uses two separate memories to provide the information storage and manipulation functions required in a digital processor. The primary memory provides the temporary register and control storage required by a digital arithmetic unit and is therefore called the register memory. The secondary memory is wired in such a way as to provide the data manipulation capability required of the logic in a digital system and is

therefore called the logic memory. A time displacement between the read-write cycles of the two memories allows them to time-share a single set of sense-amplifiers and a single set of input-output flip-flops and drivers.

The register memory is operated as a set of shift registers which are commutated once each word time by the time sequenced read-write pulse pairs generated by a P time counter. The individual registers may have from one core (as in the control registers) to n cores (as in the arithmetic registers) where n is the number of bits in a word. Commutation is controlled by the threading of the P clock lines such that the single core registers will commutate every bit time and the n core registers will commutate every n bit times. It can be seen that this mechanization is the same as that for a drum machine in which all the flip-flops are written on the drum. The number of registers therefore dictates the number of sense-amplifier/flip-flops required by the machine. The register memory timing sequencing is therefore "read register," "do logic," "write register." The "do logic" portion of the bit cycle is the only point of interest in this contract.

The "do logic" is implemented in the logic memory. The logic memory is an unusual type linear select system in which the inhibit windings thread through the memory cores in such a way as to produce a logical relationship between the input and output information rather than the duplicative relationship of normal memories. In its simplest form the write and read clocks thread every core in the logic memory so that during write clock time all the uninhibited cores are switched to the "one" state and during the read clock time all cores are reset to the "zero" state. The total bit time clock sequence is therefore: read register, write logic, read logic, write register. This is shown graphically in Figure 1.1. The flip-flops (sense amplifier, flip-flop, inhibit switch combination) are required to remember the read information for only the quarter of a bit time between the read clock pulse of one memory to the write clock pulse of the other. A block diagram illustrating this system is shown in Figure 1.2.

In the logic memory each inhibit line may be loaded with as many cores as required to implement the logic and each core may be linked by as many inhibit lines as necessary to ensure that it performs its specified logic function. The inhibit

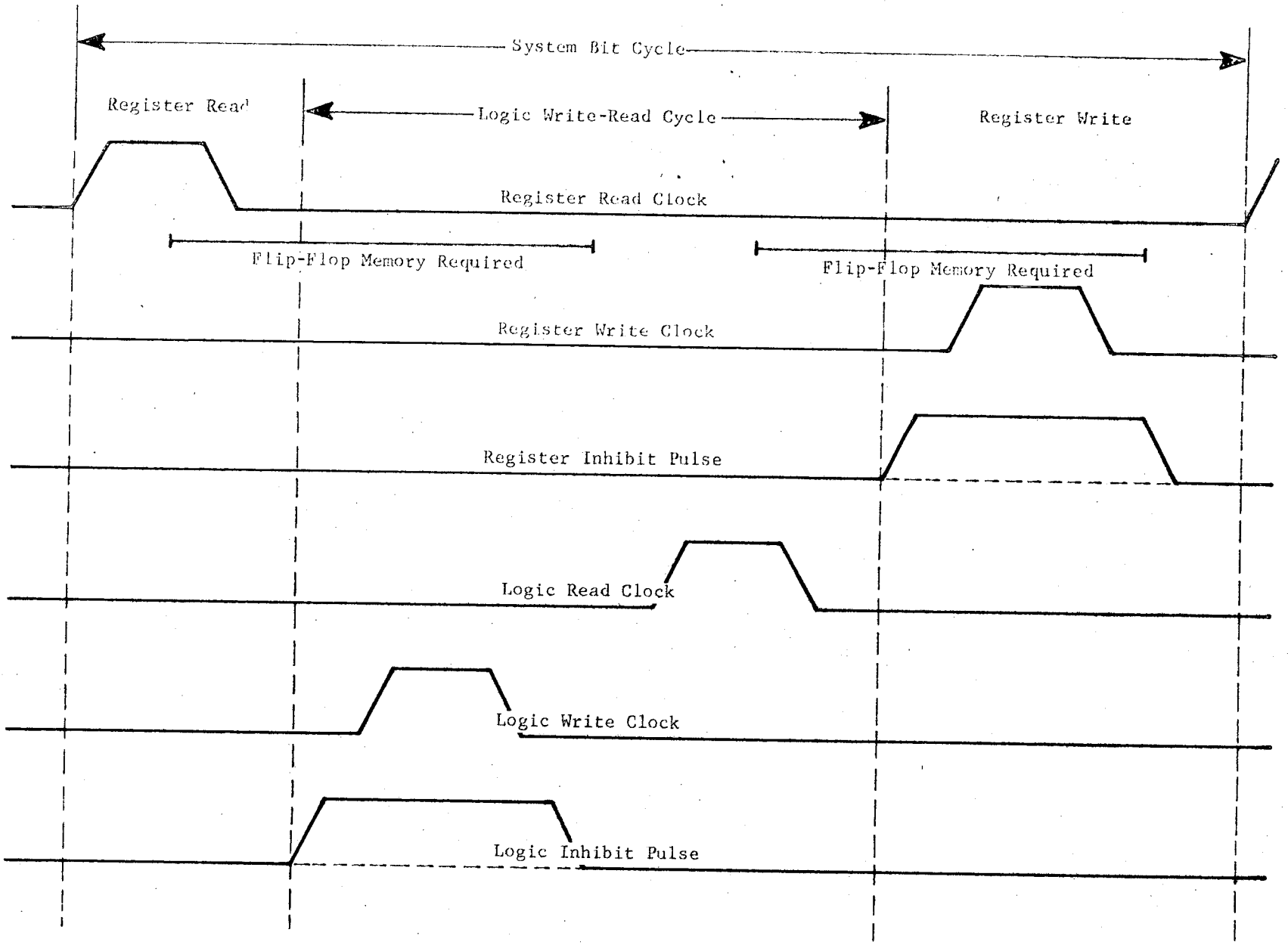

FIGURE 1.1 RELATIVE TIMING OF BIT CYCLE CURRENT PULSES

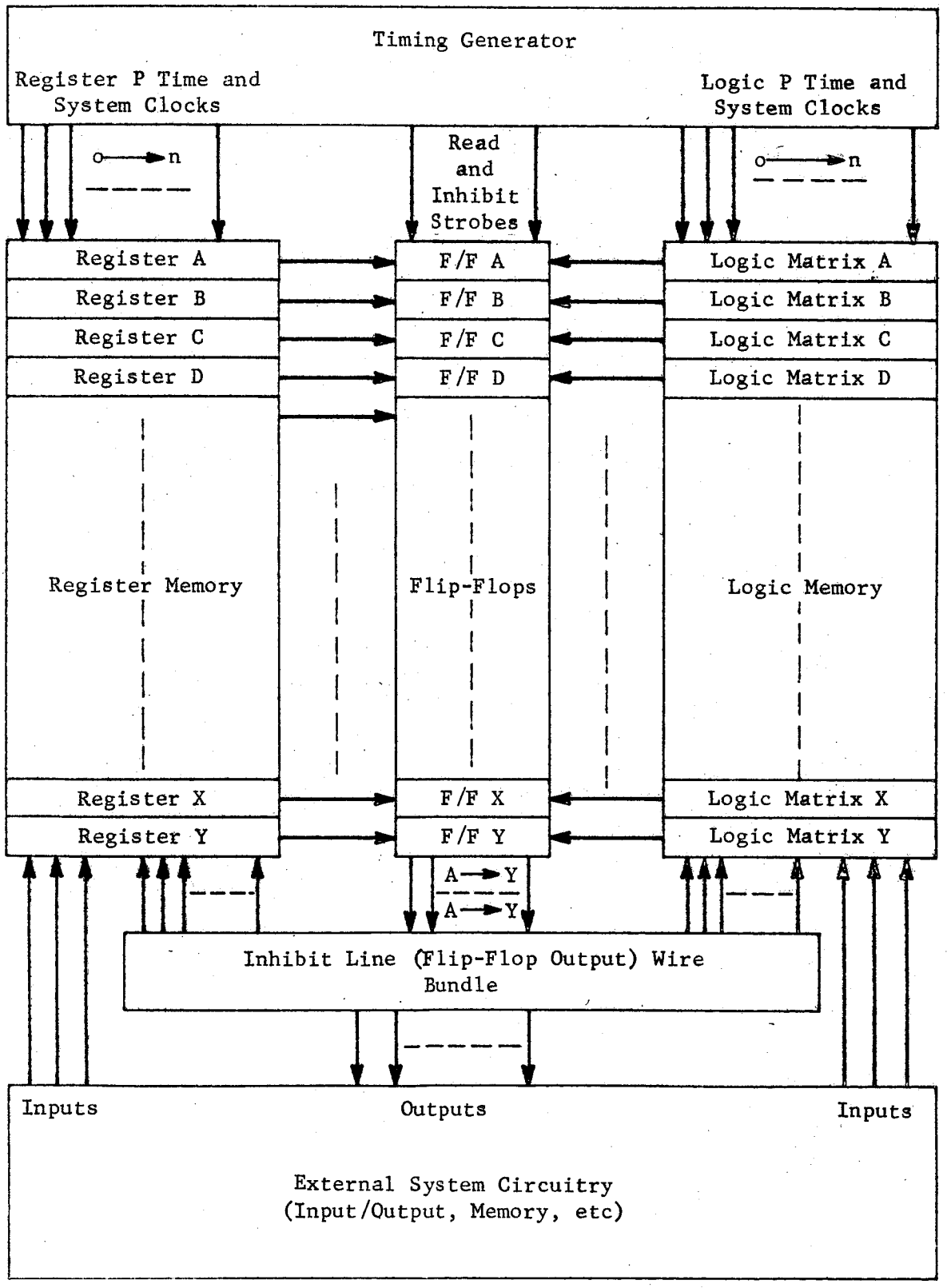

FIGURE 1.2 INHIBIT CORE LOGIC COMPUTER BLOCK DIAGRAM

line load limit is reached mechanically when the number of cores through which a signal may be reliably threaded is reached and it is reached electrically when the driving point impedance of the line exceeds that for which a current driver may be reliably and economically designed. The number of wires which may be threaded through a core is mechanically limited by the size of the wire, the inside diameter of the core, and the efficiency of utilizing hole area to its theoretical capacity. The electrical limit to the number of inhibit lines which may be routed through a core is achieved when the possible number of activated lines begins to interfere with core switching characteristics. These limit situations will determine degree of success in achieving the contract goals.

1.2.1 Idealized Logic Core Characteristics

A set of core characteristics which would be most desirable from the standpoint of system mechanization will be established in order to provide some basis of comparison between what may be achieved theoretically and what is actually accomplished. The general design limitations can be extended by the use of a core which has the characteristics listed below:

1) Low switching current threshold
2) Major loop saturation at a current level very close to the switching threshold
3) Good switching characteristic stability with temperature
4) Large inside diameter; small outside diameter
5) Insulated surfaces
6) Non-abrasive surfaces
7) Smooth beveled corners
8) Good mechanical strength and pressure insensitivity.

2. RECOMMENDATIONS AND SUMMARY OF STUDY

2.1 Recommendations

If JPL is to seriously consider further development of an inhibit core logic spacecraft computer, Nortronics strongly recommends that the steps listed below be incorporated into the development program at the earliest possible date. The studies conducted under this contract have proved beyond a doubt that the present mechanization cannot possibly hope to yield a usable system. To salvage the inhibit core logic concept will require not only drastic changes in the hardware under development but also a radical change in design philosophy.

1) Change the logic core to a 1/8 mil 4-79 molybdenum Permalloy tape-wound bobbin core.

2) Conduct a complete feasability study of inhibit core logic mechanizations centered around the tape-wound bobbin core. During this study the parameters whose limit values will be required during the design phase must be determined. The optimum system organization for the task required should also be established.

3) Embark on a conprehensive core test program which will establish system operating points, buy-in test specifications, and component design specifications.

4) Determine a set of comprehensive rules which will place the final circuit design process on a firm and consistent footing.

5) Redesign the entire inhibit core logic system using only those circuit topologies which will yield to analytical treatment.

6) Modify the package recommended in this report to the degree required to optimize the system around the improved mechanical properties of the metallic tape-wound bobbin core.

At the end of step 2) it is recommended that an analytical comparison be conducted between inhibit core logic and conventional or microcircuit logic mechanizations to determine that the benefits of the magnetic approach actually outweigh the deficiencies.

In Nortronics' opinion the steps outlined above provide the only direction open for salvaging the proposed magnetic spacecraft computer. This plan, if followed, should yield a system which displays the utmost in reliability, maintainability, and reproducibility.

2.2 Summary

The original goals established at the beginning of the JPL Inhibit Core Logic Study Contract soon proved to be unattainable. The major factor leading to this unfortunate result was the specification by JPL of a ferrite core for use as the basic logic element. The properties of this device led to difficulties in almost every area of study. Some of the problems, as in the core test specification study, proved to be insurmountable under the conditions established in the contract. The result of this study alone indicated that the proposed core logic approach could only yield an unsatisfactory system.

A reevaluation of the contract should have been discussed at the end of the core test specification study. This was not possible because of a communications breakdown between Nortronics and JPL from mid-December to mid-January. The program was therefore continued as originally planned. In order to accommodate the ferrite core into a reasonably reliable and reproducible system, many costly compromises were introduced. The results and recommendations which are presented in the various sections of this report are considered to represent an adequate and, in some cases, optimum solution to the problems as specified by JPL. However, they should not be used to formulate a judgment of inhibit core logic systems in general.

The study has proved three significant propositions. First, the present JPL system can not possibly be expected to operate satisfactorily using the presently specified logic core and current program. The core test section of this report demonstrates this fact beyond a doubt and generally suggests some of the reasons for that conclusion. The results of the tests conducted rendered the generation of a logic matrix specification which could guarantee an output signal-to-noise ratio greater than 1:1 an impossible task. It was therefore pointless to complete a core test specification for the ferrite core. It is recommended that a 1/8 mil 4-79 Molly-Permalloy tape-wound bobbin core be substituted for the ferrite core as the basic logic element. The characteristics of the metallic tape core approach the properties desired of the logic device so closely that the substitution could probably be made without requiring any system changes. A direct substitution is not recommended, however, since a full utilization of the advantages of such a change could not be taken. A complete redesign around this improved device is considered highly desirable, if not mandatory, if development is to be continued.

The second point is that inhibit core logic can be optimumly organized to achieve the full benefits inherent in this type of mechanization. The sense line, inhibit line, and clock line organization presented in Sections 3 and 4 is felt to be the optimum configuration obtainable under the conditions of the contract. The optimization was considered mainly in terms of the wiring process rather than the electrical requirements. Considerable improvement could be achieved in a situation in which more tolerance is allowed in the selection of the logic device. The entire program should be reexamined if the recommended logic core change is made. It is important that organization be studied in terms of the whole system rather than a portion at a time. Optimization criteria should be established during the feasibility study phase of the program rather than after the design is complete. It is recommended that before a total redesign is started, the entire area of feasibility and advantage be reexamined. It is not obvious at this point that inhibit core logic has any area in which it can compete favorably with standard transistor, resistor and diode techniques. It is further recommended that the optimization criteria which cover organization be established under this study.

The third area of significant accomplishment was in the packaging study. The package recommended in Section 4 of this report represents what is considered an optimum solution to the problems encountered. The system presented should be generally applicable to any ferrite core mechanization. A minimum of additional work is required to adopt the recommended change to metallic tape-wound cores. The cost of fabrication could be reduced by the elimination of the stress relief pins required in the present system, by an improved core mounting structure recessing the cores into the board, and by the obvious alleviation of core wiring processes. The electrical improvements would be equally dramatic since a larger diameter wire could be accommodated and true core-to-core wiring could be incorporated without further complicating the wiring process. It is therefore recommended that the package presented in this report be modified to the degree required to optimize the mechanical aspects of the system around the improved properties of the metallic-type core.

3. LOGIC MEMORY ELECTRICAL SPECIFICATIONS

3.1 Logic Core Test Specifications

The purpose of the core test program is to study the switching parameters of the various types of ferrite cores considered for the logic device of the Inhibit Core Logic system under the electrical, thermal and mechanical environment anticipated in the final assembly package. The test data will provide information concerning the worst-case switching parameters of the cores and will be a basis for the preparation of the purchase and incoming test specifications.

3.1.1 Ferrite Core Characteristics

The type of ferrite core selected by the engineering personnel of the Jet Propulsion Laboratories for the logic memory device is an 80-mil coincident current device requiring a full select current of approximately 350 ma - turns under coincident current operation. The core manufacturer's specifications guarantee certain switching parameters for this device at the specified operating point and at a temperature of 25° C only. The data contained in these specifications provides no information concerning the core switching characteristics over wide variations of temperature and drive current. Further, these specifications contain no information that may be used to predict the drive current at which the core can be guaranteed to achieve major loop switching. Since the current program that the cores will be subjected to in the Inhibit Core Logic system (see Appendix A) is not a coincident current pattern, the manufacturer's specifications are of no value in determining whether or not the 80-mil ferrite core is suitable for this particular application.

Before testing the device to the given current program, there are a few simple tests that may be performed which should determine the suitability of the device to the application. The most important of these tests is the measurement of the switching coefficient, Sw, and the switching threshold, F_o, of the core over the

anticipated temperature range. The switching coefficient, Sw, is generally determined by measuring core switching time, T_s, at various amplitudes of drive currents. If the core is switched from one remanent state to the other, the time required for flux reversal is proportional to the reciprocal of the excess driving field as shown in Figure 3.1. This relationship may be written as

$$Sw = T_s (H - H_o) \qquad (1)$$

where, using the notation of Menyuk and Goodenough:[1]

Sw is the switching coefficient

T_s is the switching time

H is the applied magnetic field

H_o is the threshold field.

Equation (1) predicts a single-valued switching coefficient and threshold field; however, other investigators[2] have shown that these parameters are dependent upon the manner in which the core is reset.

The switching coefficient may be determined by two methods:

1) where I set = I reset

2) where I reset = a constant >> I set (measurements are made at I set time).

Typical switching curves for an 80-mil ferrite core are shown in Figure 3.2. The curves are shown for I reset = I set and I reset = 8 amp-turns. From an inspection of Figure 3.2, certain facts are immediately evident. The curves are identical above a certain value of reset field. Below this intersection point the switching time of the core is dependent upon the amplitude of the reset driving field. Since the switching time is not constant for a given value of set current

[1] N. Menyuk and J. B. Goodenough, J. Appl. Phys. 26, 8 (1955)

[2] R. H. Tancrell and R. E. McMahon, J. Appl. Phys. 31, 5 (1960)

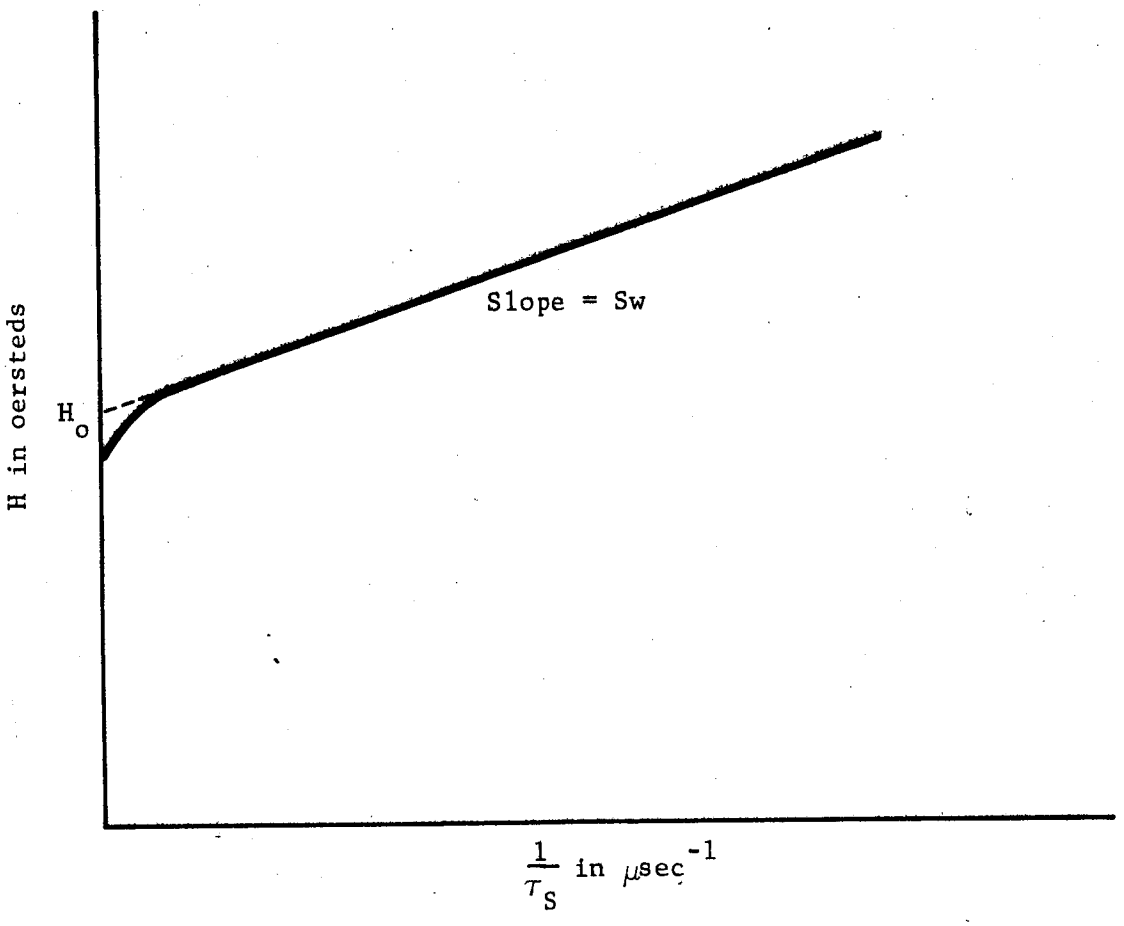

FIGURE 3.1 INVERSE SWITCHING TIME VS MAGNETIC FIELD INTENSITY FOR A SQUARE HYSTERESIS LOOP MAGNETIC TOROID

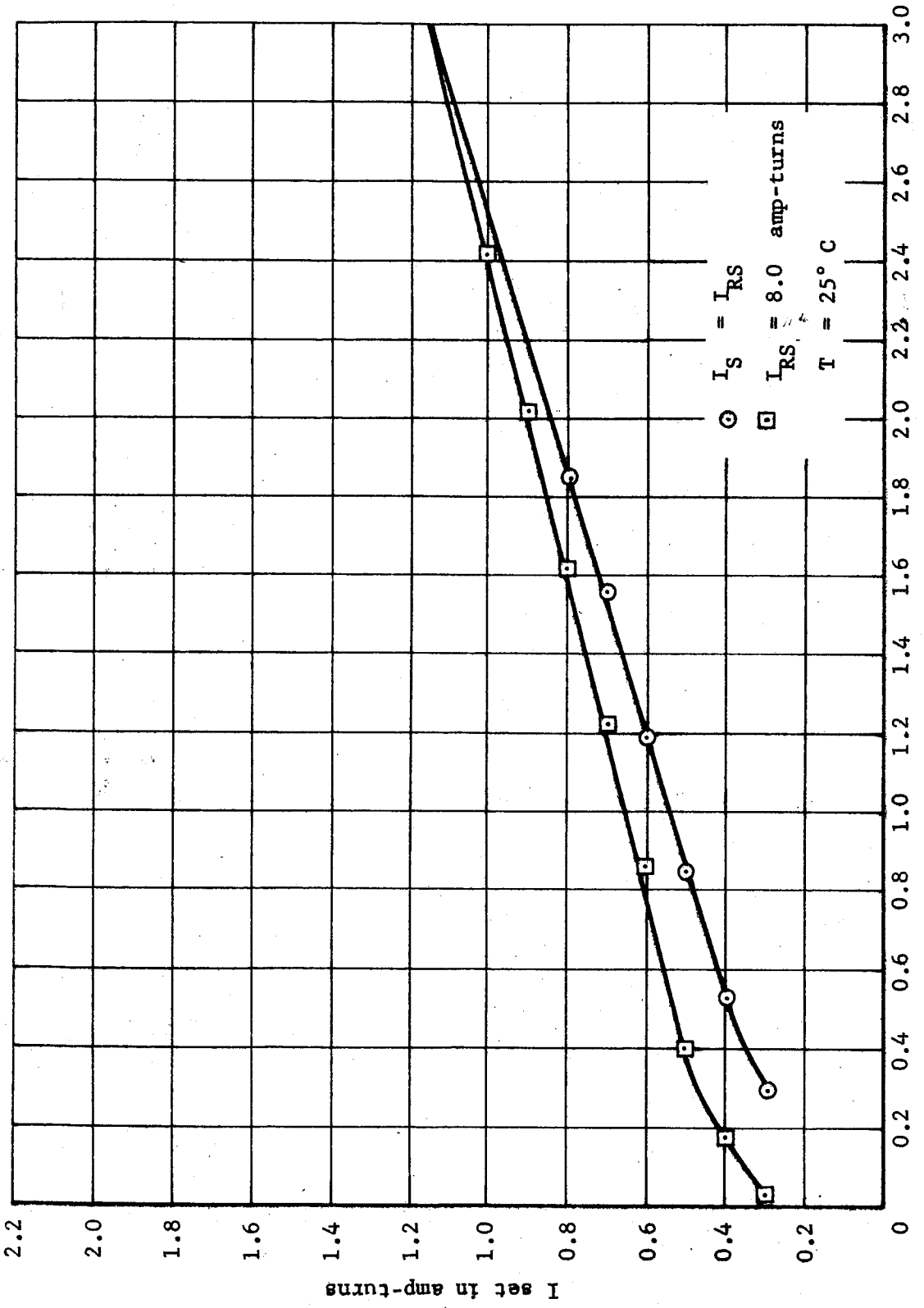

FIGURE 3.2 INVERSE SWITCHING TIME VS DRIVE IN AMP-TURNS

below the intersection point, it may be concluded that the core is operating on minor loops which are dependent upon the amplitude of the reset field. Therefore, the switching parameters of the core will also be dependent upon the reset current. These effects will become even more pronounced with wide temperature variations. Typical curves for an 80-mil core at temperatures of -10° C and +85° C are shown in Figure 3.3. For the Inhibit Core Logic system considered by the Jet Propulsion Laboratories, the inhibit current pulse performs the function of a varying reset current pulse. The amplitude of the inhibit pulse may vary from zero to 8 amp-turns. Therefore, the switching characteristics of the "one" and "zero" signals will not only be dependent upon temperature and clock current variations, but also upon the number of active inhibit terms per core. A series of tests to verify this effect will be described in Paragraph 3.1.2.

It is of interest to note that the above-mentioned effects are common to all coincident current ferrite cores of the 50-mil and 80-mil varieties. The manufacturer's recommended operating point is specified on a minor loop to increase switching speed and improve squareness. The major loop, however, is not reached until the drive current is three to six times the coincident current full select value.

3.1.2 Program Tests

The suitability of any storage device for a particular application can be determined only by an adequate device test program. The results of the test program will serve a twofold purpose. First, the engineering personnel will become familiar with device characteristics and limitations and, secondly, the test results will become a basis for the preparation of purchase and test specifications. The latter is extremely important because the manufacturer's specifications are not usually written to guarantee device characteristics over wide variations of current program and temperature. The end results of the program will be the determination of all core parameters required to establish an adequate set of final system and circuit design rules.

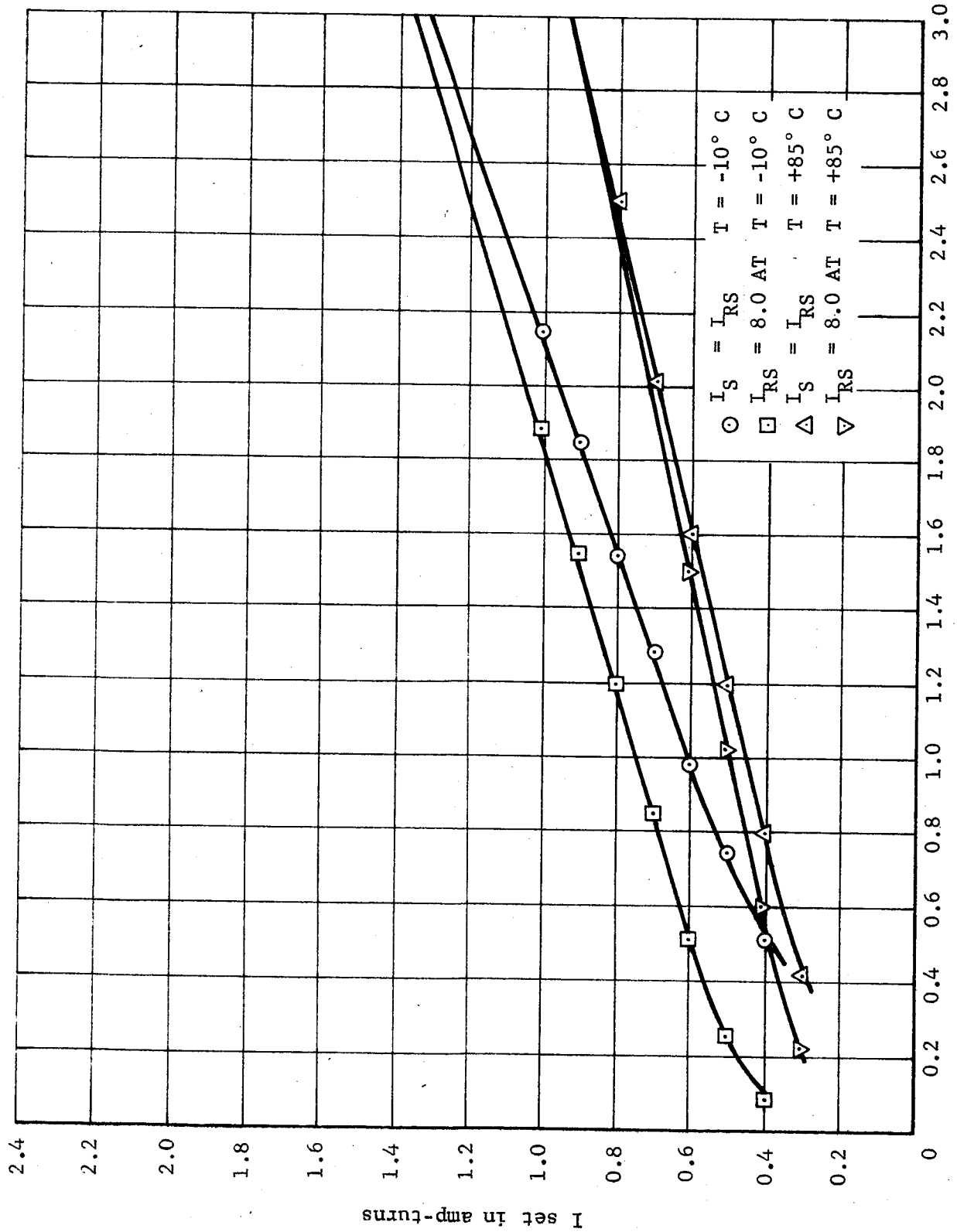

FIGURE 3.3 INVERSE SWITCHING TIME VS DRIVE CURRENT IN AMP-TURNS

3.1.2.1 Evaluation Samples: The engineering department of the Jet Propulsion Laboratories informed Nortronics personnel that specific types of ferrite cores were under consideration for use as the logic device of the Inhibit Core Logic system. These core types were Ampex 802-40, Lockheed 80-04, and EMI 82-100. Prior to the test program, considerable difficulty was encountered in obtaining samples of the Ampex and Lockheed core. EMI delivered a type 81-104 core in lieu of the 82-100 unit. Ampex had no samples of the 802-40 unit available at the time of request and procurement was therefore considerably delayed. These types of cores are low demand units and procurement time even for large orders may vary considerably. Fifty units of the Lockheed core and 91 units of the EMI 82-104 core were available at the commencement of the test program. The Ampex cores were delivered too late to be integrated into the test program. Since the number of evaluation samples was low there exists some doubt as to whether the results of this program are representative of the core types tested. The lot-to-lot variations may be even greater than those noted in the program.

3.1.2.2 Selection of Control Samples: To minimize the amount of test time, a min-max sample lot, defined as the control sample, was selected from the total number of cores. The control sample was selected by subjecting the cores to the nominal JPL current specification (see Appendix A). Units which exhibited both minimum and maximum switching parameters of the "one" and "zero" signals were selected for this sample. The results of this test are included in Appendix A. The control sample (seven units, three 81-104 cores and four 80-04 cores) was then utilized for the remainder of the tests.

3.1.2.3 Determination of Signal-to-Noise Ratio: The suitability of the ferrite core as the logic device in the Inhibit Core system is determined by the minimum signal-to-noise ratio of the core and the maximum average delta noise (ΔuV_Z). The core signal-to-noise ratio will be defined as the ratio of minimum uV_1 to the maximum uV_Z at uV_1 peaking time. The delta noise will be defined as the maximum difference of uV_Z from core to core at uV_1 peaking time. These parameters will determine the sense line signal-to-noise ratio of a logic matrix.

For an n core matrix, the sense line of which is wound for core against core shuttle noise cancellations, the sense line signal-to-noise ratio at a particular temperature will be:

$$S/N = \frac{uV_{1\ min} - uV_{Z\ max} \pm \frac{(n-2)}{2} \Delta uV_Z}{\pm \frac{n}{2} \Delta uV_Z} \qquad (2)$$

The minimum acceptable S/N ratio is generally assumed to be three to one. However, even with this S/N ratio, the sense amplifier design is not an easy task. To provide some insight to the S/N ratio problem, consider a matrix containing 50 cores where ΔuV_Z is one millivolt and uV_Z is four millivolts. To achieve a three to one S/N ratio requires a minimum uV_1 signal of:

$$uV_1 \geq S/N \left[\pm \frac{n}{2} \Delta uV_Z \right] + uV_Z \pm \frac{n-2}{2} \Delta uV_Z$$

$uV_1 \geq 103$ mv if the memory is maintained at a constant operating point.

The switching coefficient curves shown in Figures 3.2 and 3.3 indicate that the core switching time and, therefore, the core peaking time will be dependent upon the ambient temperature and amount of reset current. Thus, the S/N ratio in the Inhibit Core Logic system with a varying inhibit current program is further complicated by peaking time variations. The signal-to-noise ratio that the sense amplifier must perform to is the ratio of the minimum V_{1L} to the maximum V_{0L} at a selected strobe time. Since the minimum V_{1L} and maximum V_{0L} may occur at different temperatures, the sense amplifier which must discriminate against V_{0L} but detect V_{1L} under all conditions may require an even more stringent discrimination system than indicated by Equation (2).

3.1.2.4 Core Switching Parameters Versus Write/Read Program: Appendix B contains a series of tests which were conducted to determine the variations of uV_1 and uV_Z with temperature and write/read current program. At temperatures of -10° C, +25° C and +85° C the switching parameters of uV_1 and uV_Z were

measured subjecting the control sample cores to the minimum and maximum charge programs. The minimum and maximum charge programs are defined in Appendix B. This minimum charge program occurs with:

$$I = I_{min} \quad (570 \text{ ma})$$

$$t_R = t_{R\ max} \quad (0.6\ \mu\text{sec})$$

$$t_F = t_{F\ max} \quad (0.2\ \mu\text{sec})$$

$$t_W = t_{W\ min} \quad (1.8\ \mu\text{sec})$$

The maximum charge program contains the above parameters at the other extreme of the current driver specification. The uV_1 tests were conducted with $I_R = I_W$ = min Q and $I_R = I_W$ = max Q. The uV_Z parameters were measured for two consecutive read pulses over the conditions discussed. At -10° C with the minimum charge program the control sample units were not switching to completion. The oscillographs shown in Figure 3.15 demonstrate this fact. This is further corroborated by the decrease in amplitude of consecutive zeros. The core is operating on a minor loop and switching is limited by the duration of the current pulses under the minimum charge program. Because minor loop operation was indicated by the test results of Appendix B, a series of tests were conducted to determine what effect the inhibit current pulse would have on the uV_1 signal.

The tests shown in Appendix C were conducted with $I_i = 0$ and $I_i = 2$ amp-turns. These tests were conducted at -10° C and +85° C with various current programs. Application of the inhibit pulse had a severe effect upon uV_1 and T_p. At -10° C T_p varied between 0.73 μsec (I_W = min Q, I_R = max Q, I_i = 2 A-T) and 1.26 μsec (I_W = max Q, I_R = min Q, I_i = 2 A-T), uV_1 between 65 millivolts ($I_R = I_W$ = min Q, I_i = 2 A.T.) to 162 millivolts ($I_R = I_W$ = max Q). Again, incomplete switching was observed. Core C exhibited the minimum uV_1 signal and this core was utilized for the remainder of the tests.

Since the switching parameters of core C were severely affected by a 2-amp inhibit pulse, a more detailed uV_1 test was conducted where I_i was varied from 0 to 8 amp turns. (See Appendix D.) The tests were conducted at -10° C only.

The peaking time of core varied from 0.6 μsec to 1.12 μsec. The amplitude of uV_1 varied from 43.5 mv to 139 mv. Figures D.2, D.3 and D.4 of Appendix D are graphs of uV_1 versus I_i. The waveforms in Figures 3.14 through 3.18 demonstrate the extreme sensitivity of the uV_1 signal to the inhibit current amplitude.

Since the test results at this point in the program indicated that considerable difficulty would occur in obtaining an acceptable S/N ratio due to incomplete flux reversals, it was decided to omit the remainder of the uV_1 tests and to proceed with uV_Z measurements.

The first series of uV_Z measurements were performed on Core C at -10° C. The first test consisted of a 10-step write/read program where the write pulse of step 2 is off simulating one unit of inhibit current. With I_R = min Q and I_W = max Q, the amplitude of uV_Z was approximately 24 millivolts and irreversible flux switching was observed. In simpler terms, flux remained in the core from the previous cycles which gave the zero voltage the switching shape of a small "one" signal. Next, the write pulse of step 1 was turned off, thereby reading the core twice. The second uV_Z (read at step 2) was approximately seven millivolts. As other write pulses were turned off for the remaining steps of the program, the zero noise was observed to decrease to approximately four millivolts.

The second test consisted of a 10-step write/read program where an inhibit pulse of eight amp-turns was energized at various steps in the program. The zero noise varied from approximately 1.5 millivolts due to reversible flux switching to 28 millivolts due to irreversible switching. A complete description of these tests is contained in Appendix E. The oscillographs shown on Figures 3.14 through 3.18 demonstrate the extreme sensitivity of uV_Z to the write/read and inhibit program.

At this point in the test program it was evident that the sense line signal-to-noise could not be guaranteed to be better than one to one. Formal testing was, therefore, discontinued and samples of various other 80-mil coincident-current cores were tested to the worst-case uV_1 and uV_Z current patterns to see if there were any which would yield usable characteristics. These correlation tests are

described in Appendix F. The decrease in amplitude of uV_1 with I_i = 8 amp-turns and the high zeros were observed for all units tested. A General Ceramics unit exhibited a single-core signal-to-noise ratio of less than one to one under these conditions.

3.1.3 Evaluation of Test Results

The test results described in Paragraph 3.1.2 have verified that: 1) the type of core selected as the logic device (a coincident-current ferrite memory core) and 2) the JPL current driver specification will not provide a usable signal-to-noise ratio for the Inhibit Core Logic system.

The characteristics of the uV_1 and uV_Z signals are severely dependent upon the write/read current driver tolerances, the number of active inhibit terms, and the ambient temperature. The maximum uV_Z signal of the control sample observed was 27 mv with a peaking time of 0.78 μsec. The minimum uV_1 signal observed was 43.5 mv with a peaking time of 0.78 μsec. Thus, the minimum core signal-to-noise ratio is 1.6 to 1. The delta noise or the maximum difference of uV_Z amplitude was dependent upon the current program. If the core is subjected to the current program shown in Figure 3.4a, the amplitude of uV_Z decreases with successive read current pulses. Typical values for uV_Z (1), (2) and (3) are 27 mv, 7 mv, and 5 mv. The peaking times of these uV_Z signals were between 0.7 and 0.8 μsec. If the core is subjected to the current program shown in Figure 3.4b, the amplitude of uV_Z decreases to 1.7 mv with a peaking time of 0.6 μsec. This extreme variation of uV_Z represents a serious problem in the design of a logic matrix sense line configuration. Consider a matrix containing 64 cores with a common sense line which has been threaded for delta noise cancellation. Delta noise cancellation is generally accomplished by "bucking" core against core or rows of cores against rows of cores. With a maximum average delta noise of 1 mv per cancelling core pair the uncancelled noise would appear as ±64/2 or ±32 mv. If one of the cores is switched to a "one" the read output signal would be the algebraic sum of the uV_1 signal, one uncancelled uV_Z signal, and 31 delta noise signals. Thus, the uV_1 signal amplitude may be decreased by the uncancelled uV_Z signal and the total delta noise. The process is illustrated in Figure 3.5.

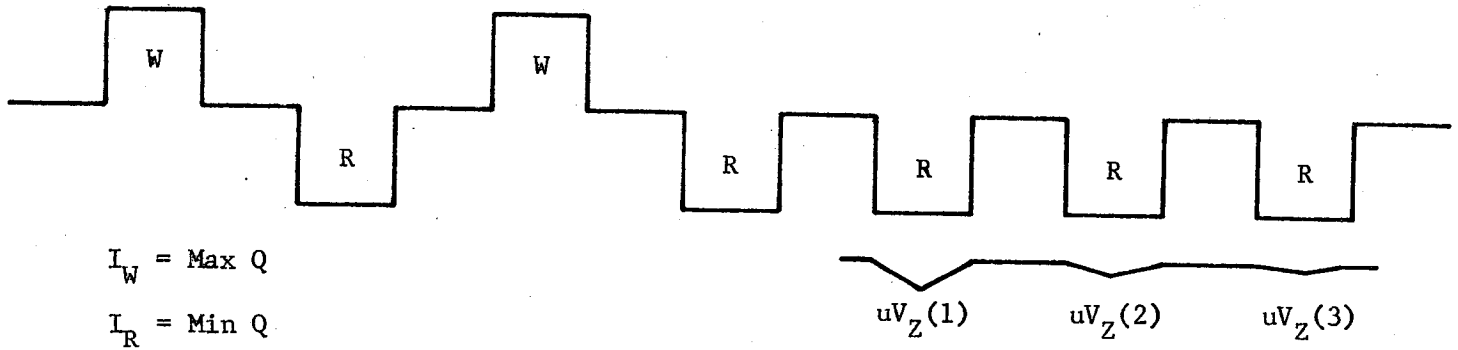

FIGURE 3.4(a) uV_Z TEST PROGRAM

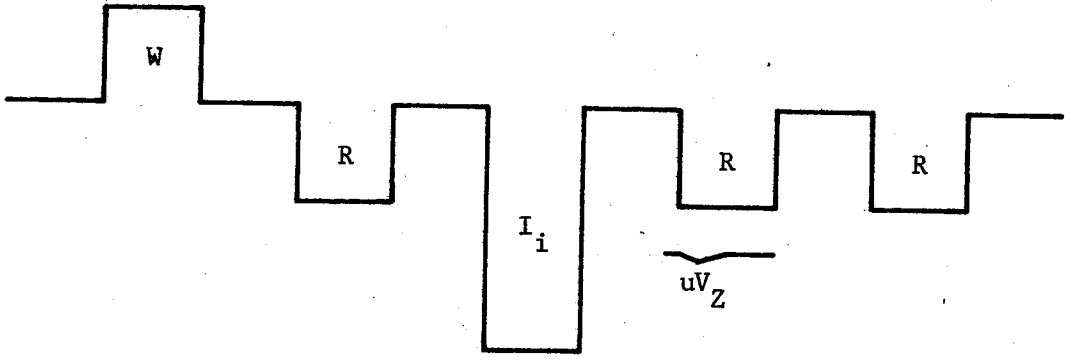

FIGURE 3.4(b) uV_Z VS INHIBIT TEST PROGRAM

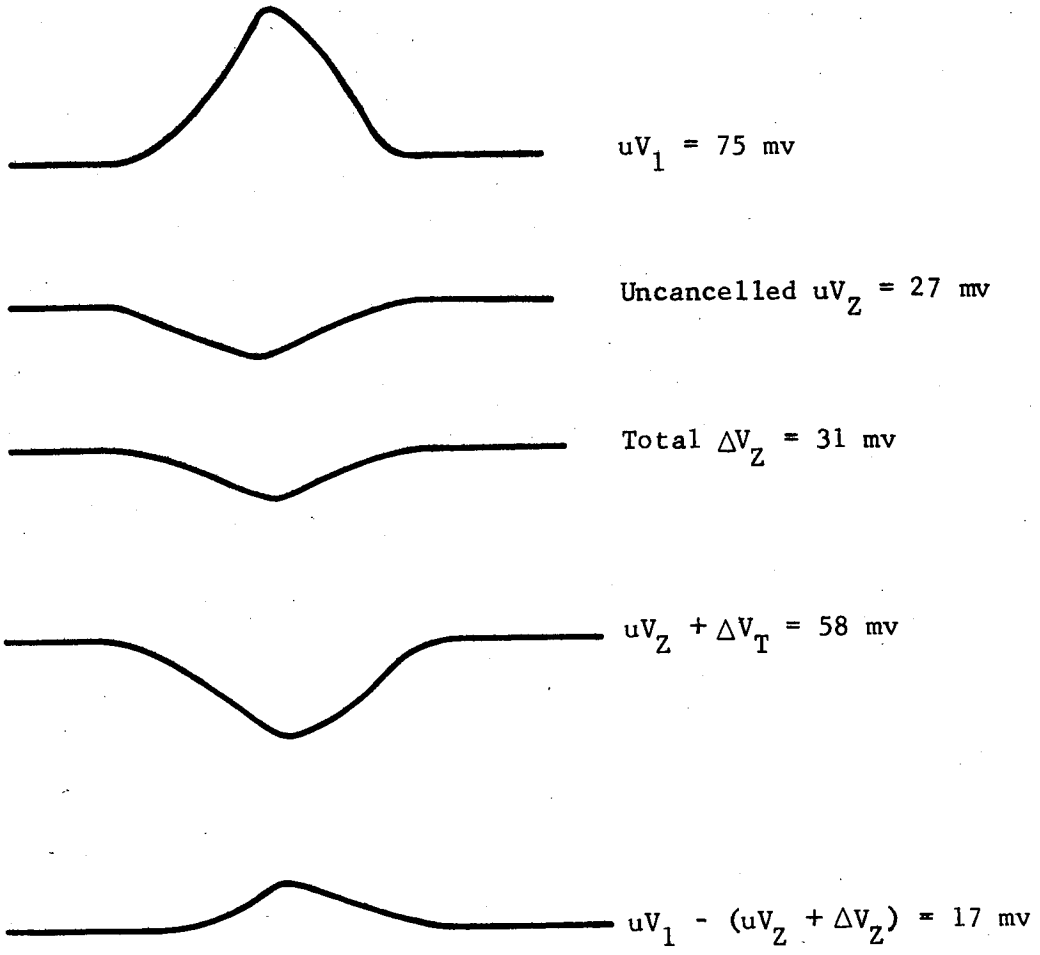

FIGURE 3.5 SENSE LINE WAVEFORMS SHOWING DEGRADATION OF uV_1 SIGNAL

With the measured values of uV_Z and delta noise of the control sample, it would be impossible to guarantee a 1-to-1 signal-to-noise ratio for any size matrix. Therefore, the 80-mil coincident-current ferrite core selected for this system is judged totally unsuitable as the logic device operating in the manner prescribed in the JPL current driver specification.

The prime cause of the poor signal-to-noise is the instability of the hysteresis loop traversed during various write/read cycles. Consider the idealized hysteresis loops of a ferrite core shown in Figure 3.6. There exists one major loop and many minor loops. At -10° C major loop operation for the 80-mil ferrite cores studied in this program is achieved with drive currents of four amp-turns and above. With $I_R = I_W = 0.6$ AT and a current pulse width greater than the switching time of the core, the operating point is path 1-2-3-4. At -10° C the pulse width specified in the JPL current driver specification is not of a sufficient duration to allow complete switching and the nominal loop is path 5-6-7-8. With a maximum charge program for the write pulse and a minimum charge program for the read pulse, the core operates on another loop as shown by path 9-10-11-12. During the write pulse the amount of flux switched is Φ_W. The flux reversed during the read pulse is Φ_{R1} and is not equal to Φ_W because of the unbalanced current program. If a second read pulse is applied, a flux change equal to Φ_{R2} will be produced. The normal shuttle flux observed in reading a zero with a balanced write/read program would be Φ_S as shown in Figure 3.6. The flux change of Φ_{R2} is not reversible and is 15 times larger than Φ_S. This mode of loop operation produces a high uV_Z signal which has the shape of a small uV_1 signal. During the third read pulse the flux change, Φ_{R3}, is less than Φ_{R2} but still four times larger than Φ_S. After several read pulses, the operating point of the core will settle at point 13 where the flux change will be Φ_S. This process is further complicated by the variation of core parameters with temperature changes.

The variation of the uV_1 signal as a function of the inhibit current may be analyzed in a similar fashion. Consider a core operating with $I_R = I_W$ = minimum change and $I_i = 0$. The operating point is the minor loop shown as path 1-2-3-4 of Figure 3.7. As I_i is increased in steps of 0.6 AT the remanent operating

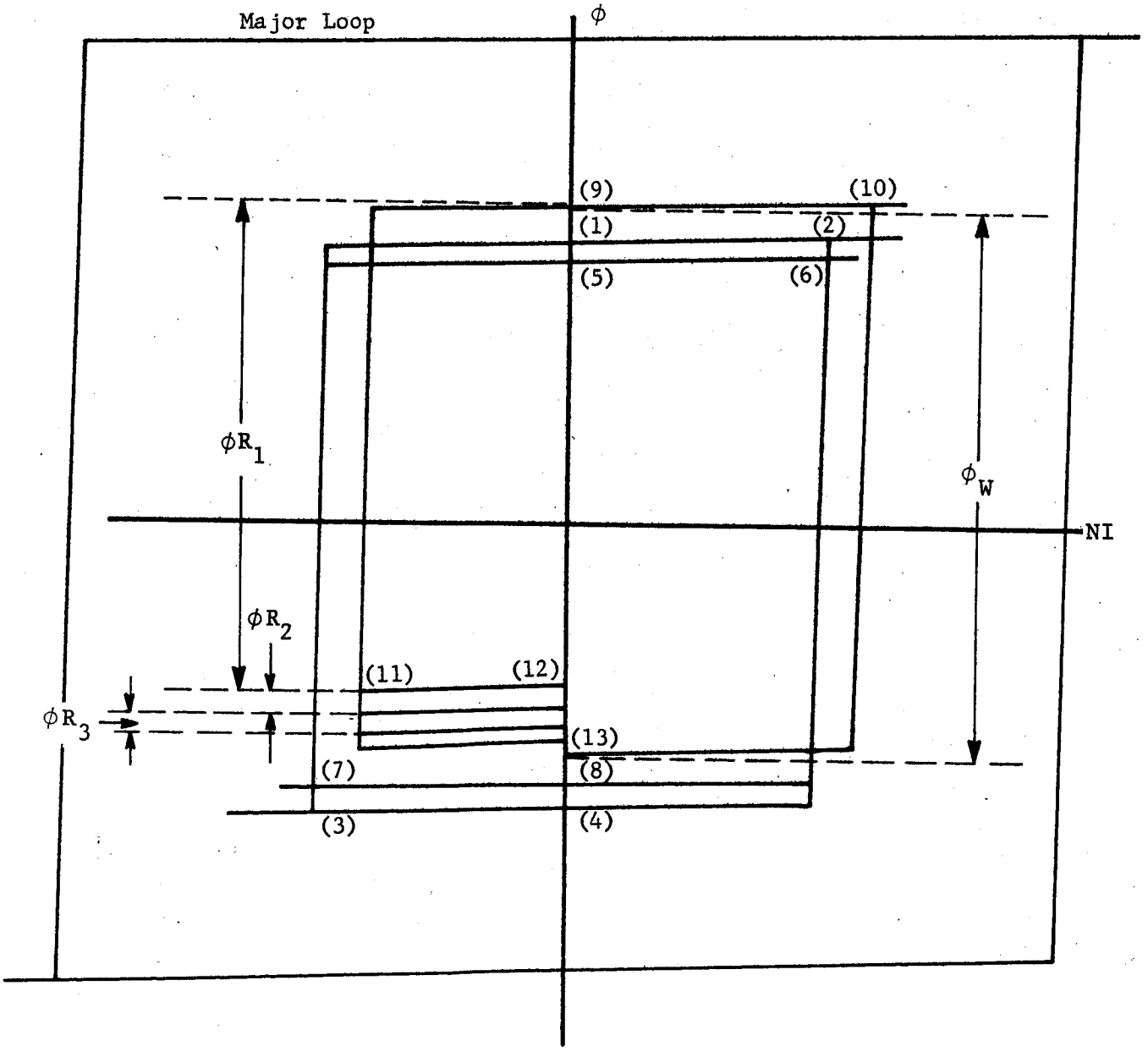

FIGURE 3.6 IDEALIZED HYSTERESIS LOOPS SHOWING NONSTABILIZED LOOP OPERATION AS A FUNCTION OF READ/WRITE CURRENT TOLERANCES

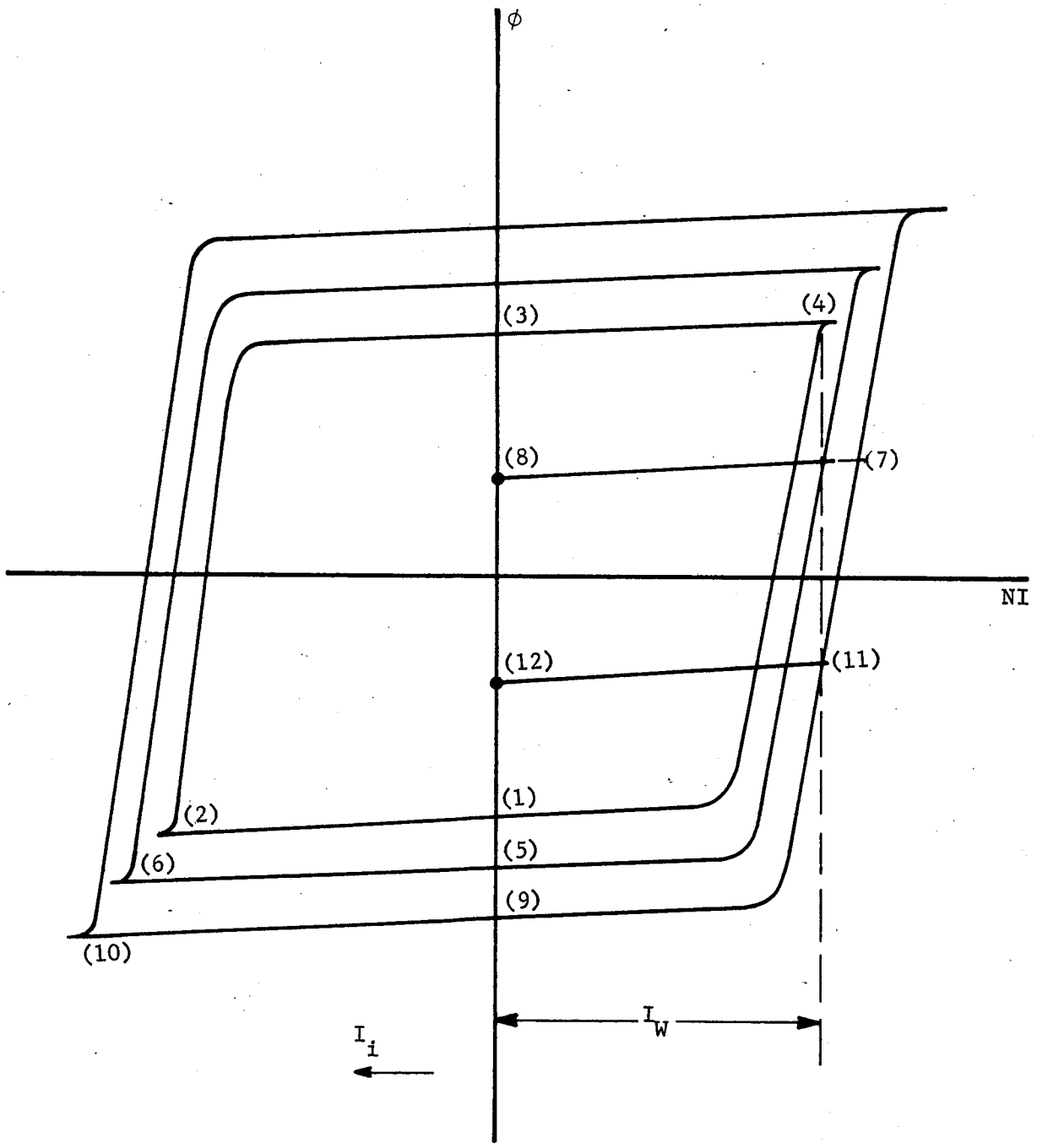

FIGURE 3.7 IDEALIZED HYSTERESIS LOOP NONSTABILIZED LOOP OPERATION AS A FUNCTION OF INHIBIT CURRENT AMPLITUDE

point is changed from point 1 to 5 to 9 etcetera. During this process the width of the loops is increasing and for the case of constant write current less flux is switched during the write pulse time. As a consequence, the uV_1 signal decreases as I_i is increased.

Eventually the major loop remanent point is reached and the uV_1 signals remain constant but considerably decreased in amplitude. The tests described in Appendix D have verified this effect. With $I_i = 0$, uV_1 was 119 mv for Core C. With I_i = 8 amp-turns, uV_1 decreased to 43.5 mv.

3.1.4 Recommendations

Paragraphs 3.1.2 and 3.1.3 have demonstrated that serious problems exist with the use of a ferrite core as the logic device in the present Inhibit Core Logic system. Before recommendations are proposed which may alleviate some of these problems, a careful consideration of the properties of an ideal magnetic core for use in the Inhibit Core Logic system is necessary to establish criteria which will determine device or system modifications. These characteristics are:

1) Major loop operation at relatively low values of drive current
2) Insensitivity of switching parameters to wide variations of temperature
3) Uniform switching characteristics from core-to-core
4) Ease of design characterization.

Any device considered for the Inhibit Core System should exhibit characteristics similar to the above. The characteristics of the coincident-current ferrite cores considered for the present system differ greatly from those of the ideal core. The point of major loop operation is not well defined and occurs at approximately 2.0 amp-turns of drive current at 25° C. A -10° C major loop operation occurs at a higher value of drive current. Noticeable changes in the switching characteristics were present with reset currents of 4 and 8 amp-turns. The switching parameters of uV_1 and uV_Z are quite sensitive to the anticipated ranges of ambient operating temperatures. The variation of uV_1, $\frac{\Delta uV_1}{uV_1\ (25°\ C)}$, between -10° C and +85° C for Core C is 0.48%/°C.

The switching time variation, $\frac{\Delta T_s}{T_s(25^\circ C)}$, for Core C is 0.48%/°C.

These values were calculated from the test results of Appendix B. Due to change in the operating point from the minor to major loops, peaking time variations are severe over the temperature range.

In general, ferrite cores exhibit nonuniform switching characteristics from core to core. At 25° C the peaking time of the 81-104 cores is specified at 1.4 ±0.4 μsec or a variation of ±29 percent. The switching time is specified for a maximum value only. Many investigators,[3,4,5,6] have proposed switching models for the ferrite core; however, the correlation between the model and the device has generally not been adequate. Further, these models were formulated under the assumption of major loop operation.

Although the ferrite core appears totally unsuitable for the application, certain modifications to the current program are indicated from the test data which might possibly produce a reasonable signal-to-noise ratio. Loop stabilization may be accomplished utilizing a reset current pulse of approximately 6 to 8 amp-turns following the read clock. The write and read clock pulse widths should be increased possibly two to three times their present value. This will insure completion of switching, thereby increasing the uV_1 amplitude. The amplitudes of the write and read clock probably will have to be increased to insure that sufficient flux is switched to provide a reasonable signal level. Whether or not these measures will produce a designable system can only be determined by a comprehensive test program.

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[3] D. Nitzan, SRI Project N 3696 November 1961

[4] E. M. Gyorey, J. Appl. Phys. 28, 9 September 1957

[5] N. Menyuk and J. B. Goodenough, J. Appl. Phys. 26, 1 (1955)

[6] V. Hesterman, Special Conference on Linear Magnetics, 1961, pp 265-292

The corrective measures described above are drastic in nature. The most desirable solution to the problem would be to utilize a type of magnetic core for the logic element, the characteristics of which approach those of the ideal device. This type of device is the metallic type wound bobbin core. Since this core is fabricated from metallic tape (4-79 Molybdenum Permalloy), it is relatively insensitive to temperature variations.

Switching curve measurements have indicated that the characteristics of the core are not affected by varying reset currents. Measured variations of uV_1 with temperature were 0.05%/°C over the range of -10° C to +85° C. Switching time variations were also 0.05%/°C. The core exhibited major loop switching at low values of drive current. A comparison of the switching curves of a typical tape-wound core and Core C of the control sample is shown in Figure 3.8. Tape-wound cores are available with uV_1 output voltages much higher than those of the ferrite core. The higher output voltage available from the switch core will result in considerable simplification of the sensing circuits. Design models for the tape-wound core which characterize reversible and irreversible flux change have been formulated and verified.

In view of the above statements, it is strongly recommended that the use of the ferrite core as the logic element of the Inhibit Core Logic system be discontinued and that consideration be given to the substitution of a metallic tape-wound bobbin core. Again, it must be emphasized that a comprehensive test program will be required to verify whether or not a reasonable signal-to-noise ratio is possible utilizing metallic tape cores.

3.2 Logic Matrix Specification

A detailed specification describing the logic matrix input and output characteristics is required to provide valid criteria for the design of the drivers, timing circuits, and sense amplifiers associated with the logic memory and also to provide adequate test criteria upon which to base final acceptance of manufactured logic modules. The initial device evaluation and system feasibility study, which must precede any serious design effort, should provide adequate guidelines for choosing the set of parameters required to fully characterize the logic matrices.

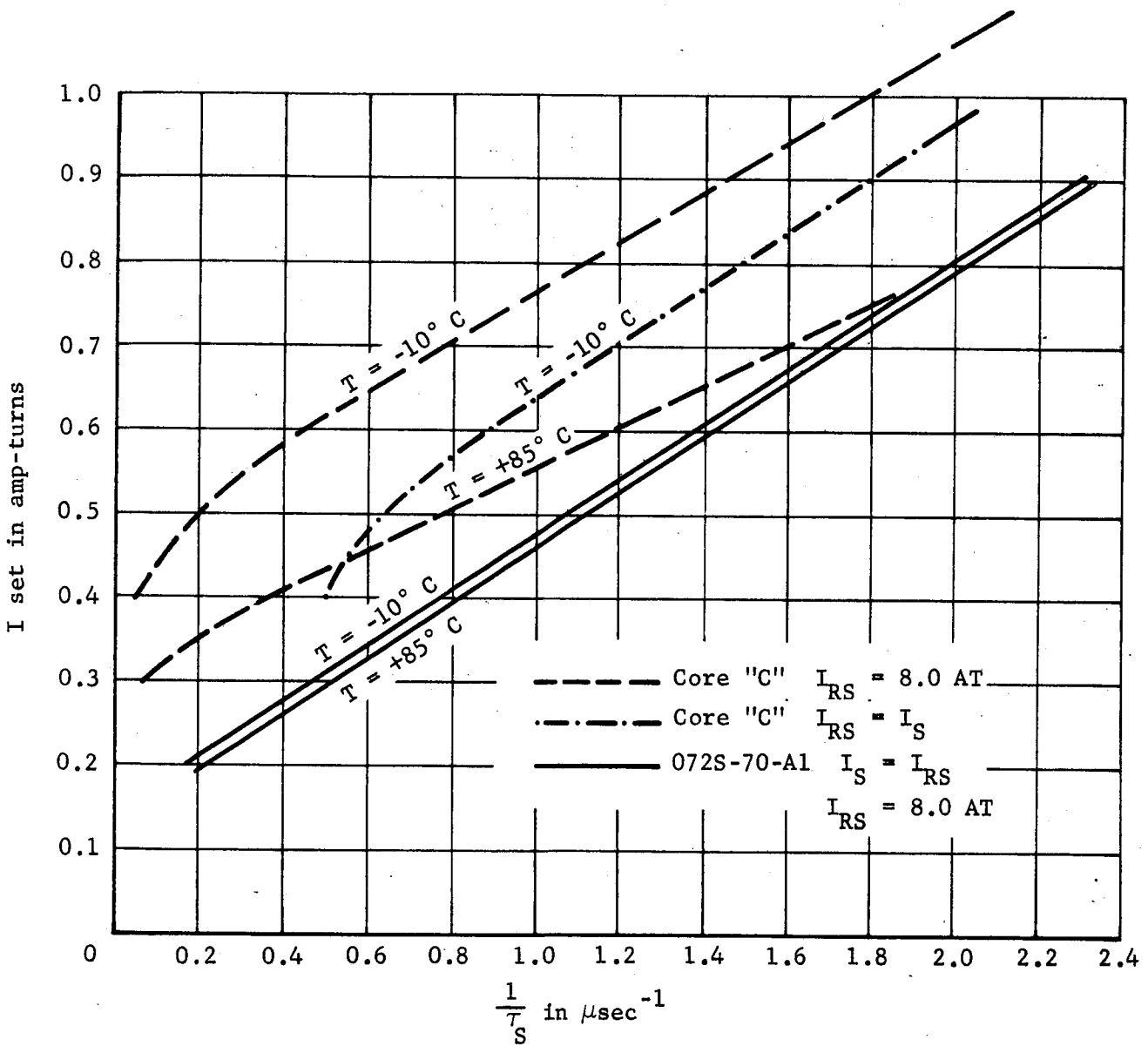

FIGURE 3.8 COMPARISON OF SWITCHING CURVES FOR CORE "C" AND TYPICAL TAPE-WOUND BOBBIN CORE

Evaluation of the required logic matrix parameters is a three-step process:

1) Establishing the basic relationships between known and measurable matrix device characteristics and the matrix specification parameters

2) Collecting and organizing enough device data to enable a reasonably accurate calculation of the limit values expected of the matrix parameters for the matrix operated throughout its specified operating ranges

3) Experimentally verify the parameter limit values calculated.

It is obviously important that both calculation and verification be based upon devices whose characteristics lie within their design specifications. Because of the impossibility of arriving at a usable specification for the ferrite core considered for the logic device in this study, the process described for arriving at a meaningful logic matrix specification could not be carried to any usable conclusion. The remainder of this section of the report will describe the work that has been accomplished in this area.

3.2.1 Logic Matrix Specification Parameters

Each of the parameters listed below must be assigned numerical minimum and maximum values for each of the logic matrices before final design of the associated memory circuitry may be started. The list is divided into four functional areas; inhibit, write, read, and sense, which are listed in the time order in which they start to occur during the logic memory write/read cycle. Each of these functional areas has been broken into two groups of parameters. Group A contains those which might be classed as independent variables since their values are determined by the core operating point and are chosen from the aspect of system operation. Group B includes the dependent variables which are forced upon the system by the choice of values for the Group A parameters. A fifth group, representing system environment parameters, has been added.

1) Logic Inhibit Pulse - I_L

Group A	Current amplitude
	Pulse width
	Rise time
	Fall time
Group B	Peak voltages required to drive inhibit lines
	Peak flyback voltages at trailing edge of inhibit pulse
	Peak crosstalk voltages and currents during rise and fall of clock pulses
	Line termination impedance

2) Logic Write Clock Pulse - C_{LW}

Group A	Current amplitude
	Pulse width
	Rise time
	Fall time
	Time duration from leading edge of I_L to leading edge of C_{LW}
Group B	Peak voltage required to drive write clock line
	Peak flyback voltage at trailing edge of write clock pulse
	Peak crosstalk voltage and current during rise and fall of inhibit and read clock pulses
	Line termination impedance

3) Logic Read Clock Pulse - C_{LR}

Group A	Current amplitude
	Pulse width
	Rise time
	Fall time
	Time duration from leading edge of I_L to leading edge of C_{LR}

Group B
- Peak voltage required to drive read clock line
- Peak flyback voltage at trailing edge of read clock pulse
- Peak crosstalk voltage and current during rise and fall of inhibit and write clock pulses
- Line termination impedance

4) Sense Line Response - V

Group A
- Geometric relationship between the sense line and the clock and inhibit lines (especially the read clock line)
- Read coupling relationship between sense line and matrix cores

Group B
- Amplitude of sense line "one" signal output
- Time relationship of "one" signal relative to leading edge of read clock
- Amplitude of sense line "zero" signal output
- Time relationship of "zero" signal relative to leading edge of read clock
- Sense line terminating impedance
- Amplitude of crosstalk voltage induced by clocks and inhibits

5) Environmental Requirements
- System operating and nonoperating temperature limits
- Shock and vibration requirements
- Radiation field intensities
- Radio noise field intensities and frequency spectrum.

3.2.2 Evaluation of Logic Matrix Limit Parameters

The most obvious method to apply to the problem of logic matrix characterization is to build the matrices as specified by the logic to be mechanized and to experimentally determine the values of the parameters required. Under tight schedule conditions, however, this method is obviously costly since final circuit design cannot proceed until all the logic modules are fabricated. A less obvious but

more detrimental effect of this procedure is that it restricts the validity of design values to a single set of modules. Overcoming this deficiency requires that a statistically large sample of modules be fabricated and tested before final circuit design begins or that the final circuits be reassessed and, if necessary, redesigned for each system. In situations of tight scheduling and in systems where reproducibility, maintainability, and reliability are prime goals, the build and test method of design is obviously unworkable.

A more reasonable approach to the problem of design parameter evaluation requires a thorough knowledge of the basic relationships between the individual element characteristics and the gross module parameters required. Since device characterization is absolutely necessary in establishing procurement criteria, the device parameters should be well known by the end of the system feasibility study phase. From the procurement criteria a set of device design limits must be established. Having established these, circuit characteristics may be evaluated analytically from a knowledge of the basic relationships between device and circuit characteristics. Methods of determining these relationships from experimental data will be discussed in some detail throughout the remainder of this section. It will be assumed that all the parameters in the A groups listed in Paragraph 3.2.1 have been specified along with all required core design value limits. It will also be assumed that the general mechanical layout of the cores, inhibit wires, clock wires, and sense wires within each module has been established. A general diagram of the logic memory write/read current program is shown in Figure 3.9.

3.2.2.1 Logic Inhibit Pulse - I_L: The voltage required to drive the inhibit lines under fixed current rise time and amplitude conditions is fixed by the driving point impedance of the line being driven and the mutual inductance between this line and all other mutually active inhibit lines. For the sake of ease of measurement and analysis, the line impedance and coupled voltages may be broken down into two components: the first is dependent only upon the wire size, material, length, and geometric layout, and the second is strictly dependent upon the core shuttle voltage per inhibit term and the number of active inhibit lines passing through each core on the line.

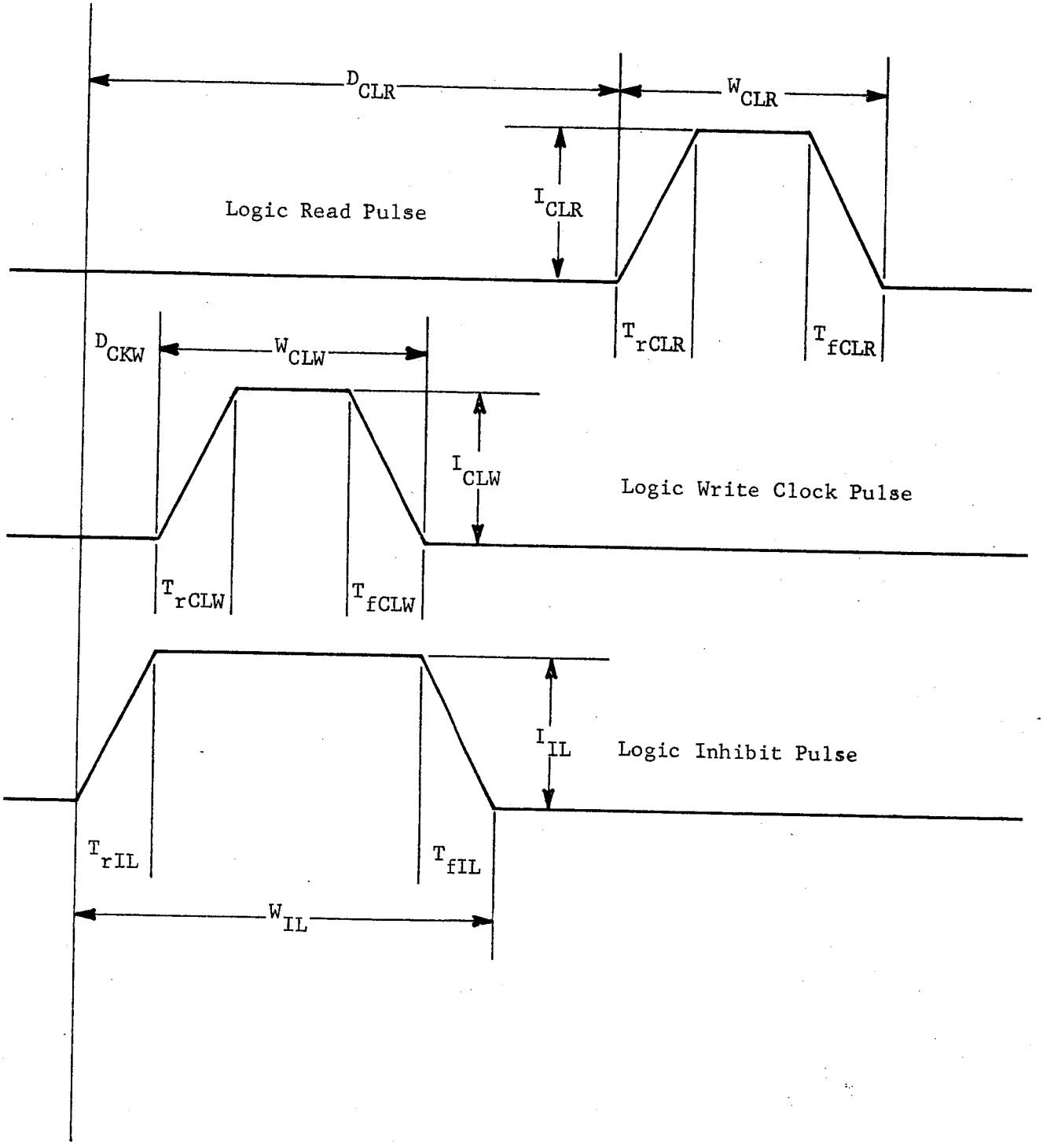

FIGURE 3.9 DETAIL OF LOGIC WRITE-READ CURRENT PULSE PROGRAM

The inhibit line self-impedance, which is composed of internal skin effect inductance, external geometry controlled inductance, static field resistance, and skin effect resistance, may be analytically calculated using well-known techniques[7] since all the constants required are set by the configuration chosen. The calculations required, however, are extremely laborious and involve approximations whose validity must be rigorously proved for each situation. Since the configuration and its tolerances are assumed to be well established, a simple set of measurements made on a well-designed test fixture can probably be justified in terms of effort and validity to accomplish the given task. Such a test fixture is described in Figure 3.10. The self-impedance test results may be made using the specified current pulse program and therefore may be directly applicable to the specification.

The voltage coupled from other inhibit lines is much more difficult to determine unless all the inhibit lines are run in a single bundle through the entire logic memory. While running the lines through the stack in this manner reduces the evaluation problem, it unfortunately maximized the value of the coupled voltage. On the basis of the final wiring layout, an empirical set of weighting functions can be worked out to relate the maximum coupled voltage for each wire to the maximum possible value for a worst-case wire. The worst-case mutual inductance can also be measured on the test fixture shown in Figure 3.10.

The core shuttle voltage contribution to the inhibit drive voltage (due to the change in current in the line being driven) can be evaluated directly from a core count and the core output zero voltage evaluation data. The total problem is not quite as simple as this, however, since each core may also be inhibited by as many as 12 other inhibit lines. A careful study of the logic and a further evaluation of the shuttle voltage characteristics at various pulse current levels and rise times is required to determine valid final design values. The problem is not as insurmountable as it may seem at first if it is assumed that all possible flip-flop states can be expected. A simple tabulation and count method can be devised to yield the desired worst-case situations. This could be easily programmed on a commercial computer.

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[7] S. Ramo and J. R. Whinnery, Fields and Waves in Modern Radio, John Wiley and Sons, New York, 1953, Chapters 5, 6, and 7

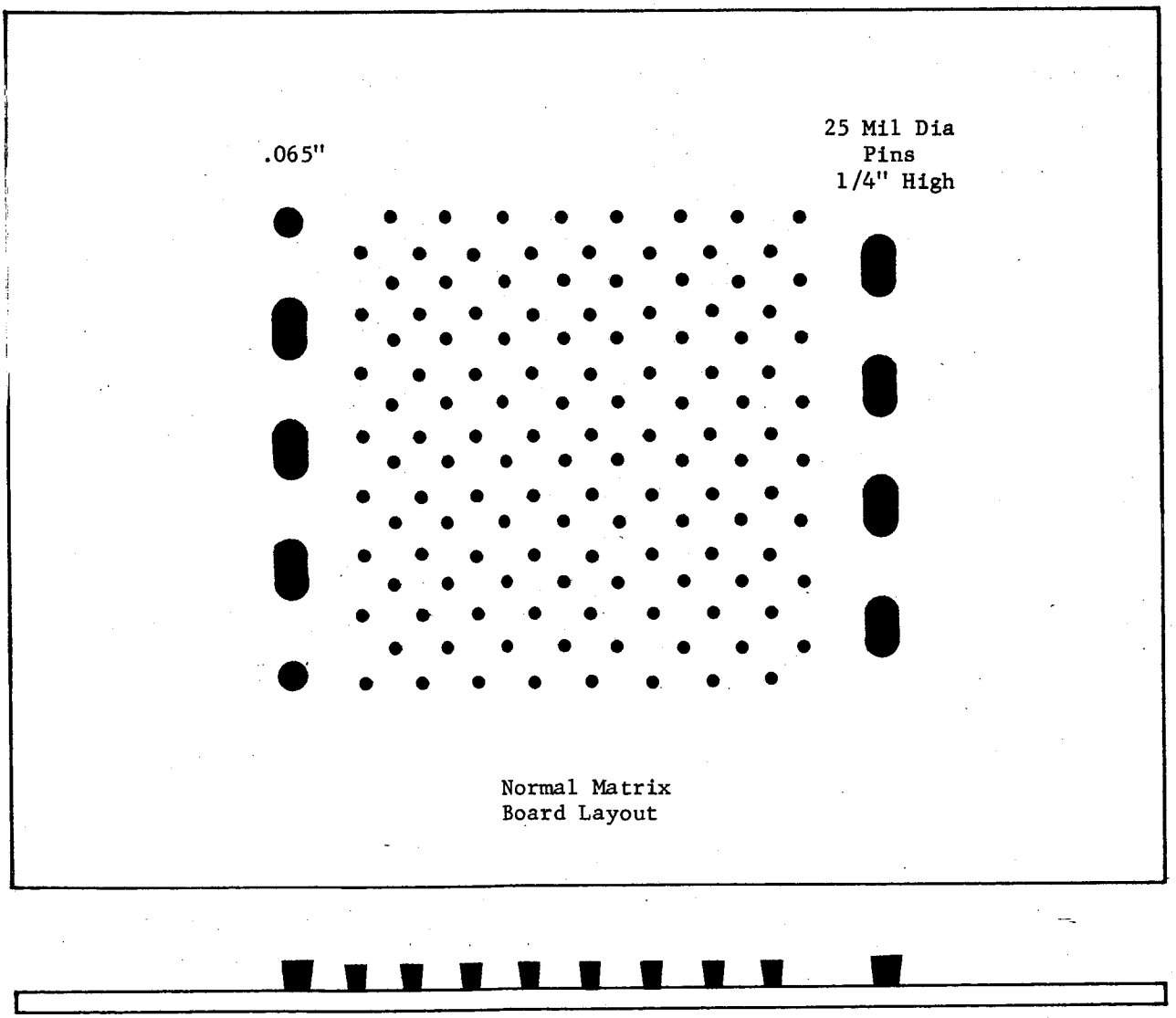


FIGURE 3.10 MATRIX WIRE CHARACTERISTIC MEASUREMENT TEST FIXTURE

The peak flyback voltage at the fall of the inhibit may be calculated in the same manner as the maximum leading edge drive voltage requirement. The wire mutual and self-inductances should be known in advance and the core response to the fall time conditions specified may be easily measured.

A sample calculation based upon the "true" inhibit output of flip-flop E is presented here as an illustrative example of the process just described. The device parameter values assumed as worst-case values are only rough estimates and should not be used for actual design purposes. The values which are noted as measured represent only average values for the final packaging configuration. The discussion of packaging configurations is contained in Section 4.

Assumed values of device parameters:

1) Wire:

A_{WG} #38 solid annealed copper

$R_{DC} \simeq 0.775$ ohms per foot measured at 85° C

$\frac{R_{AC}}{R_{DC}} \simeq 1.00$ measured at JPL operate conditions

$L_{(\#38\ wire)} \simeq$ 0.130 uh per foot measured with L.C. meter and at JPL operate point on shorted 5-foot twisted pair

$L_{(\#38\ wire)} \simeq$ 0.540 uh per foot measured with L.C. meter on 10-foot loop

$L_{(\#38\ wire)} \simeq$ 0.390 uh per foot measured with L.C. meter and at JPL operate point on module test jig

$M_{(max\ average)} \simeq$ 0.107 uh per foot measured at JPL operate point on module test jig

2) Core:

Lockheed 80-04 (JPL special)

Shuttle voltage for varying inhibit drive as shown in Figure 3.11.

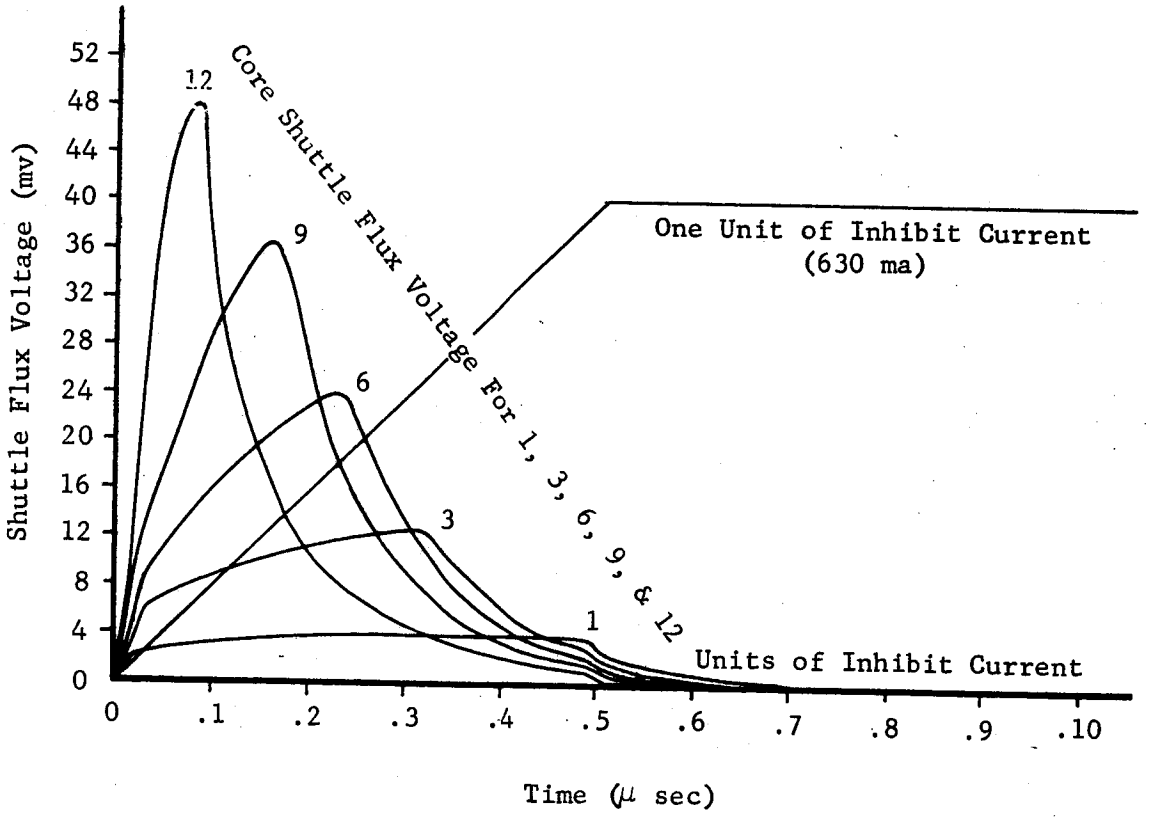


FIGURE 3.11 ESTIMATED SHUTTLE FLUX MEASUREMENTS FOR VARYING UNITS OF INHIBIT CURRENT

3) Layout:

Total number of Logic Memory Cores - 460

Number of Cores strung by E - 316

Worst-case distribution of mutual inhibit terms

No. of Cores	No. of True Inhibits
1	12
4	10
35	8
50	6
100	4
96	2
30	1

(this table represents an estimate, not an accurate tabulation)

Estimated total length of a matrix wire which links all 460 logic cores - 144 inches

Estimated length of E inhibit line - 100 inches

Maximum number of mutually active inhibit lines in the stack - 26

Number of coupling inhibit lines averaged over entire length of the E line - 4

4) Pulse Conditions:

Inhibit pulse rise time - 0.5 μs

Inhibit pulse fall time - 0.2 μs

Inhibit pulse amplitude - 630 ma

Inhibit pulse width - 4 μs

Rise and fall times are assumed to be linear

5) Results for E Line:

Total resistance	- 6.46 Ω
Total self-inductance	- 3.25 uh
Total non-core-coupled voltage	
Leading edge - 4.48 volts	
Trailing edge - 22.4 volts	
Total core-coupled voltage	
Leading edge - 4.50 volts	
Trailing edge - 22.5 volts	
Total leading edge voltage swing	- 15 volts
Total trailing edge voltage swing	- 63 volts
Total flat-top voltage	- 4.1 volts

Figure 3.12 displays a set of idealized waveforms which depict each of the contributions to the inhibit line drive voltage of flip-flop E along with a composite showing the maximum total voltage that can be expected across the line. Since line-to-line and line-to-ground capacitance was not accounted for, the actual voltage waveforms seen in the system may vary considerably from that shown in the diagram. This will depend upon how the active and inactive inhibit lines are terminated. The given figure should, however, give a fairly accurate picture of the flux load to be seen by the E flip-flop output and the flux time distribution required to maintain the specified pulse shape.

The crosstalk voltages generated on the inhibit lines by the read and write clock may be calculated in a similar manner using the known coupling constants.

The example given may be mechanized and the constants used verified by experiment. Any adjustments required in the matrix constants as a result of this step should be incorporated. Using this final set of parameters, each of the other inhibit line voltages may be calculated. The overall inhibit line design specification can then be generated. The only variables which arise in these subsequent calculations are layout parameters and weighting functions.

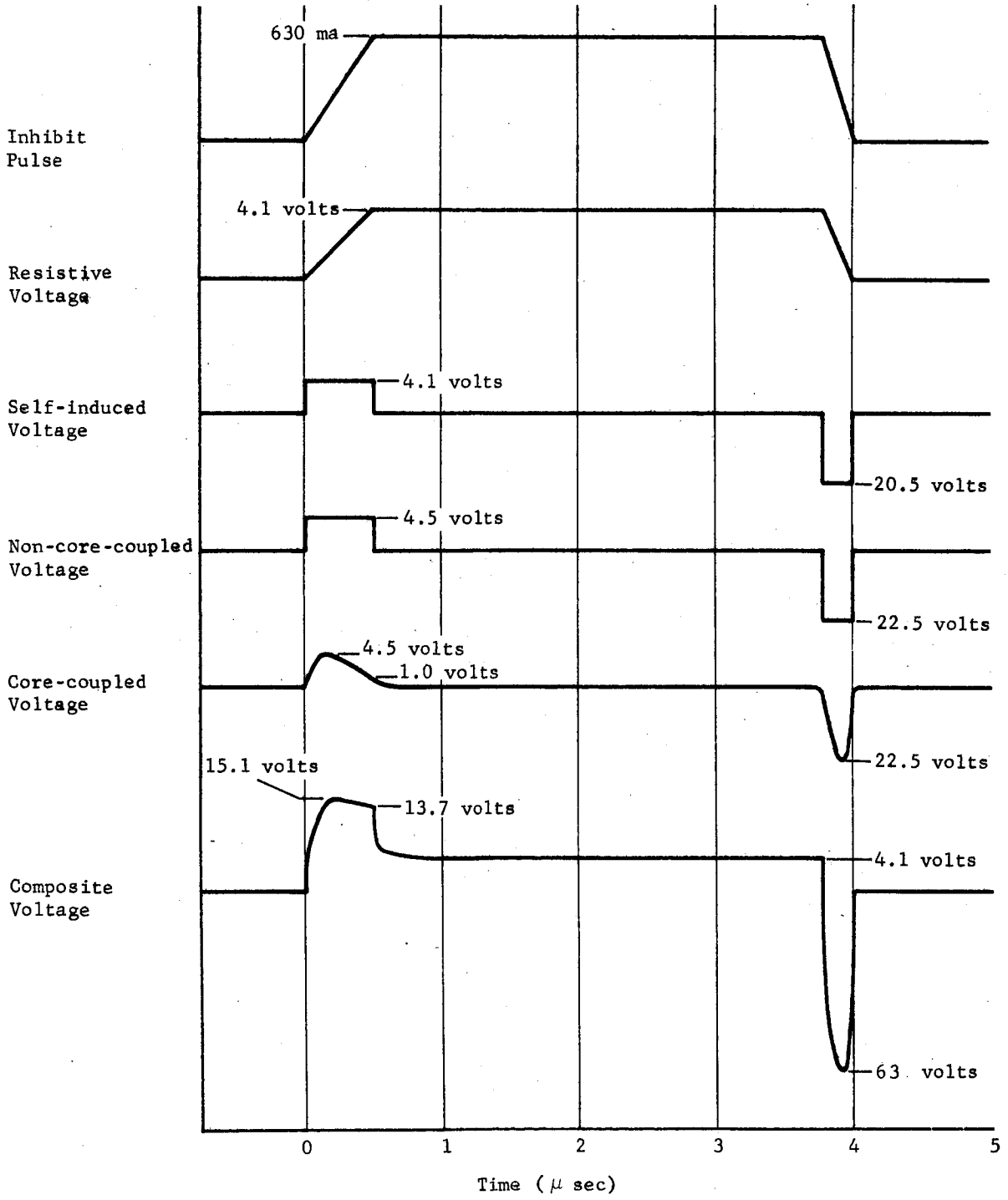


FIGURE 3.12 ESTIMATED MAXIMUM E FLIP-FLOP DRIVE VOLTAGE REQUIREMENTS

3.2.2.2 Logic Write Clock Pulse - C_{LW} and Logic Read Clock Pulse - C_{LR}: The Group B parameters required for the final design of the read and write clock drivers may be calculated in the same manner and using the same basic device parameters used for the inhibit lines. The same weighting function criteria may be used here as was used for the inhibit line calculations. The read clock calculations are simplified considerably by the fact that only the read clock lines are activated at read time. If a single read clock is used, matters are simplified even further. The write clock calculations are identical to those for the read clock if the write clocks are forced to rise after the inhibits have stabilized. However, if the write clock and inhibit lines are energized together, serious crosstalk problems may arise. Unless this is properly accounted for, the effective write clock pulse may be forced to remain off until after the inhibit lines are stabilized. If the write pulse width is the least bit critical, the final result may be to severely restrict the amount of flux written into uninhibited cores.

Sample calculations covering the read and write clock specification parameters will not be given here because of their similarity to the inhibit line calculations.

3.2.2.3 Sense Line Response - V: Since it is assumed that only one sense amplifier design will be used throughout the system, only the worst-case matrix configuration will be discussed. Because of wiring problems, the logic module has been restricted to 64 cores. This in turn limits the practical size of any logic matrix to 64 cores. The 64-core matrix will therefore be considered as the worst-case configuration (the largest flip-flop matrix, that of F_4, contemplated in the present system, contains 60 cores). Figure 3.13 shows the basic sense winding pattern developed for the relatively large matrices of the present inhibit core logic system applied to the 64-core matrix. The characteristics of this configuration which make it desirable are: ease of wiring, zero nominal flux window area, core-to-core shuttle noise cancellation along each column, and column-to-column shuttle noise cancellation along the sense line. Coupling from the read clock line to the sense line is minimized by the orthogonal relationship between these two lines. The core-to-core cancellation is achieved by canting all the

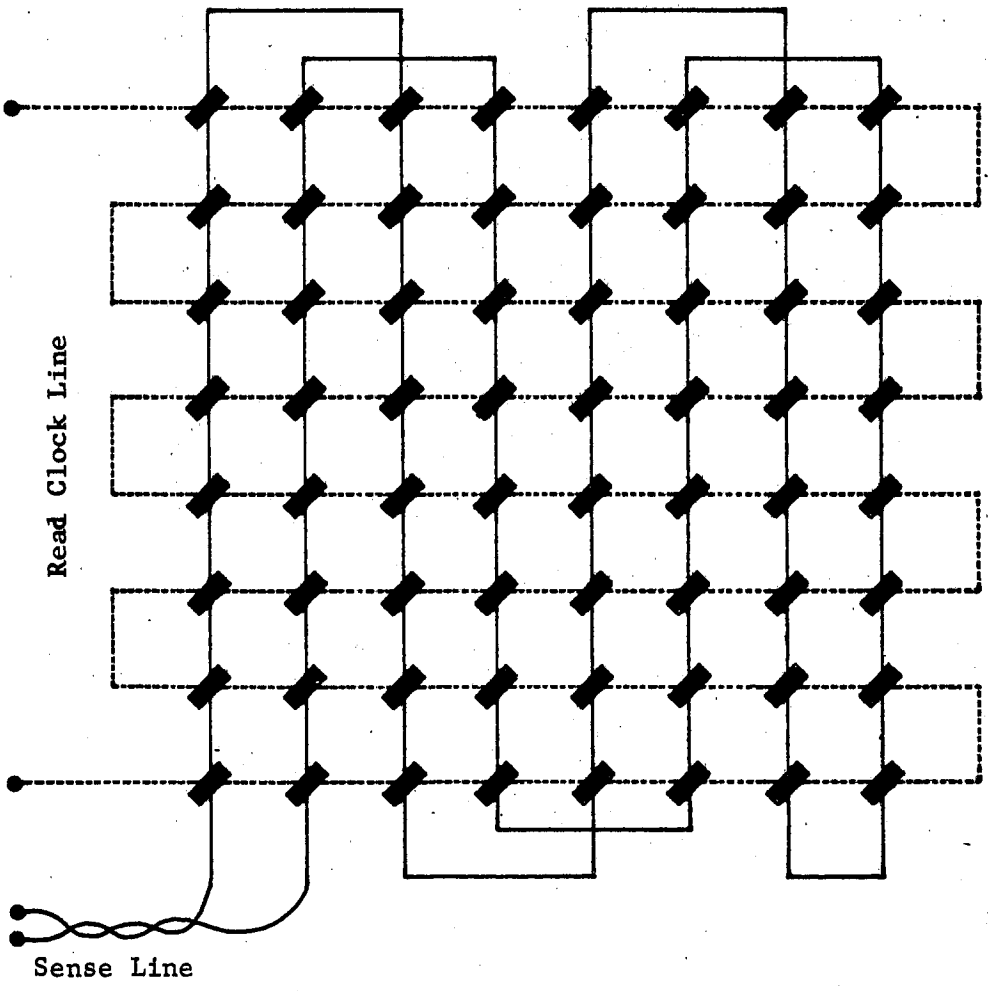


FIGURE 3.13 SENSE LINE, READ CLOCK LINE CONFIGURATIONS FOR 64 CORE MATRIX

cores in the same direction so that the read clock couples every adjacent row of cores in the opposite direction relative to the sense line.

The core test discussion covers the calculation of the sense line signal-to-noise ratio due to the core parameters. The only areas not covered are read clock line to sense line air coupling, and sense line termination.

The test fixture shown in Figure 3.10 can be used to measure the required parameters in much the same way that it was used in the inhibit line tests. The characteristics required are the limit values of the read clock to sense line mutual inductance, and the read clock or inhibit term to sense line intersection capacitance. Measurements made indicate that a mutual inductance of 3.2 n henrys and an intersection capacitance of 0.05 uuf can be expected for the 64-core matrix. From this information both the air-coupled noise contribution to the output signal-to-noise ratio and the required sense line to ground terminating impedance may be calculated. The cross sense line terminating impedance may be calculable; however, a direct measurement of the requirements is probably justifiably easier. From these considerations and those discussed under core testing come the final sense line minimum "one" signal, maximum "zero" signal, termination impedance, and common mode voltage swing values.

3.3 Conclusions

The inhibit core logic technique can evolve into a designable system assuming sufficient ground work is laid in device and geometrical configuration evaluation. The evaluation of the present system could not be completed due to the unusable device characteristics displayed by the logic core under consideration. However, certain useful conclusions and recommendations may be made in terms of the logic module and matrix specification.

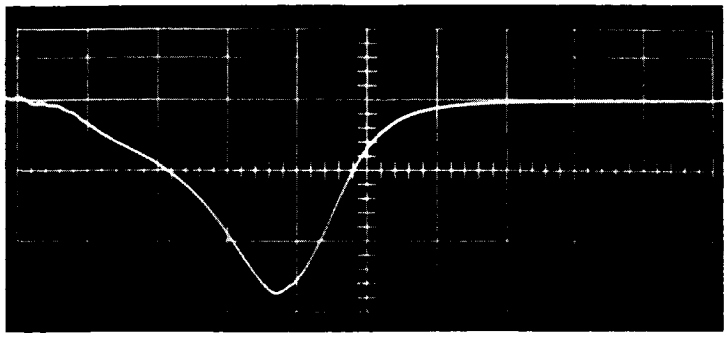
Because of the complexity of the module wiring configurations, some of the design parameter evaluation may be accomplished empirically far more easily than through dynamic field analysis. Once the configurations have been established along with

their design tolerances, a relatively simple test fixture may be built which can almost perfectly simulate actual matrix situations. If the current pulse specifications are established, the simulation experiments may be designed to yield data which may be applied directly to setting up the final specification.

Anything which can be done to reduce the complexity of the design problem without jeopardizing system performance goals should be seriously considered. Two areas of possible improvement are evident: 1) Lengthening the inhibit pulse rise time and width in order to minimize the degree of system disturbance created by inhibit switching would reduce considerably the complexity of the inhibit and write clock line specifications. Under these conditions it should be possible to cut required inhibit power by as much as a factor of two and position the write clock such that the inhibit lines are reasonably stabilized during the write clock rise time, 2) Using a single-system read clock would save at least 12 pulse time read clock wires which are now required to string through the logic memory. This would reduce read clock specification problems considerably. In the largest matrix, the F_4 flip-flop, it would introduce only five more delta noise pairs out of 25, which should be more than compensated for by the reduction in zero noise program sensitivity gained by this move.

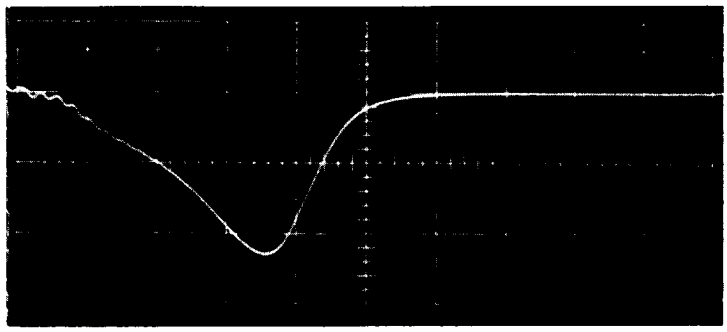
The square matrix core array is superior to a linear core array in that it allows an easy method for stringing the sense line for minimum flux window area, it allows the read clock line to sense line coupling to be minimized through an orthogonal arrangement of the wires, and it tends to reduce the inhibit line and clock line inductance over an open loop situation (0.54 uh/ft for open loop: 0.39 uh/ft for the square array). The disadvantages of the square array in the present situation arise from the fact that very poor volume efficiency is achieved because both the number of cores per array is fixed (this has been fixed by stringent assembly problems associated with the ferrite core) and the number of outside connections per array is fixed (this is obviously fixed by the logical equations). The use of a more easily wired core (a metallic tape-wound bobbin core) could allow at least a twofold increase in the number of cores per array which would result in a volume reduction of up to 50 percent.

The recommendations mentioned above should be studied again after the far more basic core device problem discussed in the core test section has been solved.



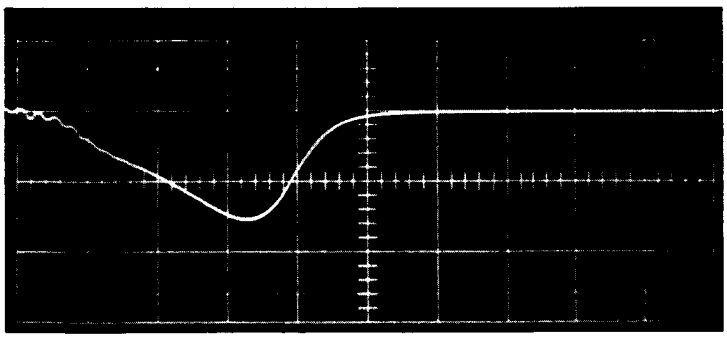
$I_i = 0$

uV_1 = 139 mr T_p = 0.74 μsec



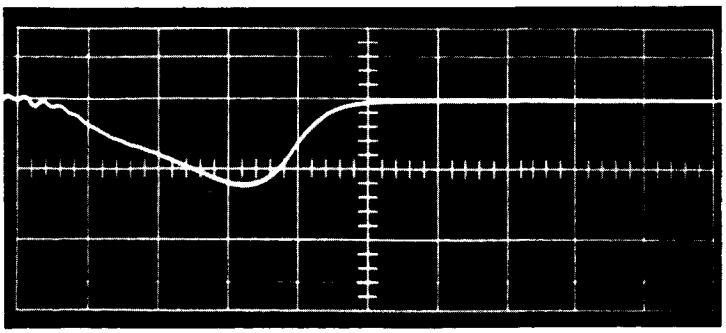
I_i = 0.6 amp

uV_1 = 115 mv T_p = 0.72 μsec



I_i = 1.2 amp

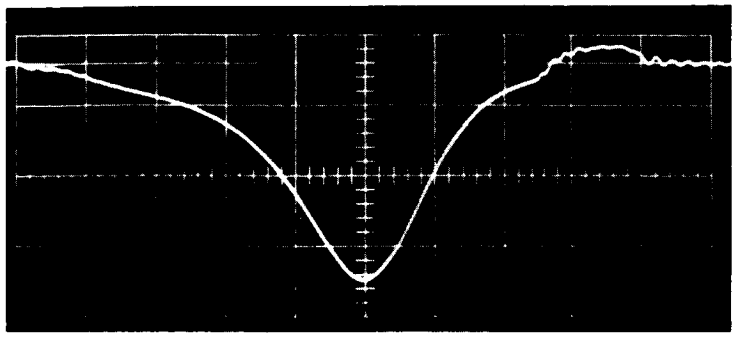
uV_1 = 76 mv T_p = 0.66 μsec



I_i = 8.0 amp

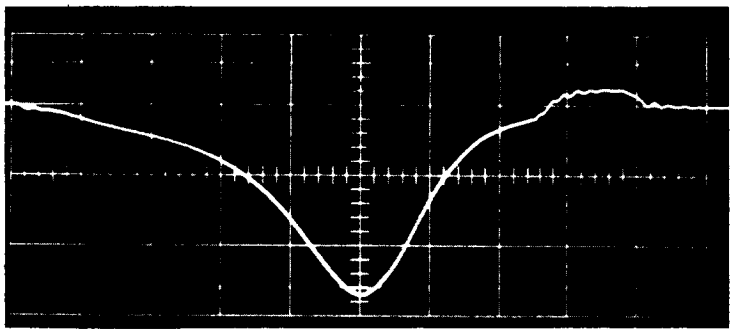
uV_1 = 60 mv T_p = 0.62 μsec

FIGURE 3.14 CORE "C" I_R = Max Q I_W = Min Q T = 10° C T = 0.2 μsec/cm



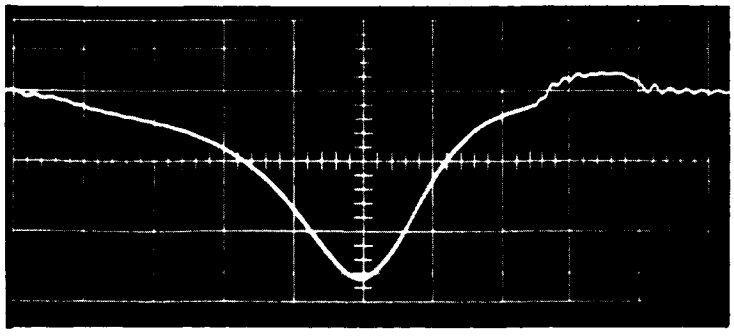
Core "A"

uV_1 = 152 mv T_p = 1.0 μsec



Core "D"

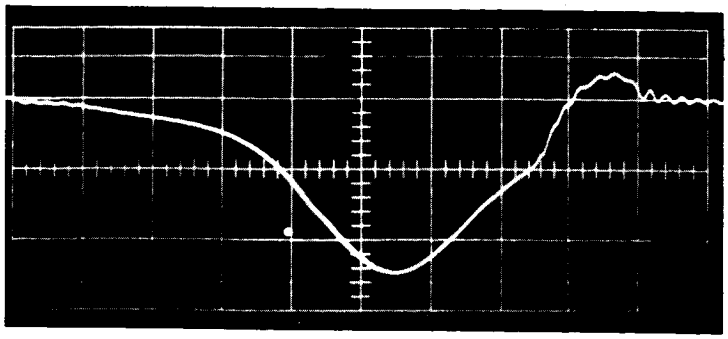
uV_1 = 136 mv T_p = 1.0 μsec



Core "F"

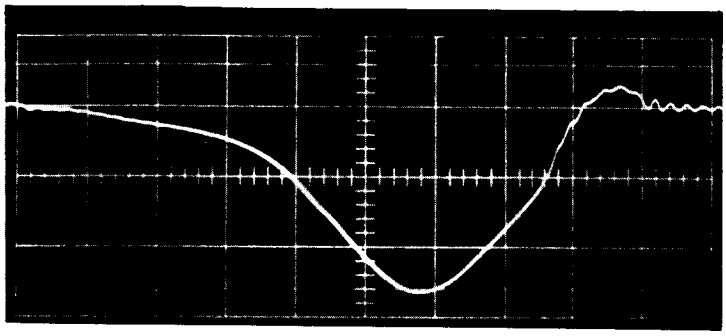
uV_1 = 136 mv T_p = 1.0 μsec

FIGURE 3.15 $I_R = I_W$ = Min Q T = -10° C T = 0.2 μsec/cm



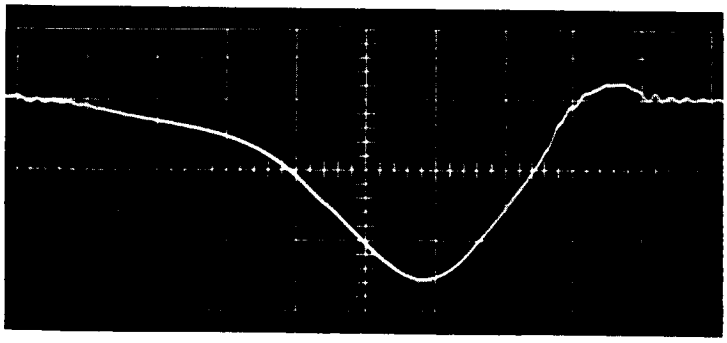
$I_i = 0$

$uV_1 = 122$ mv $T_p = 1.1\ \mu$sec



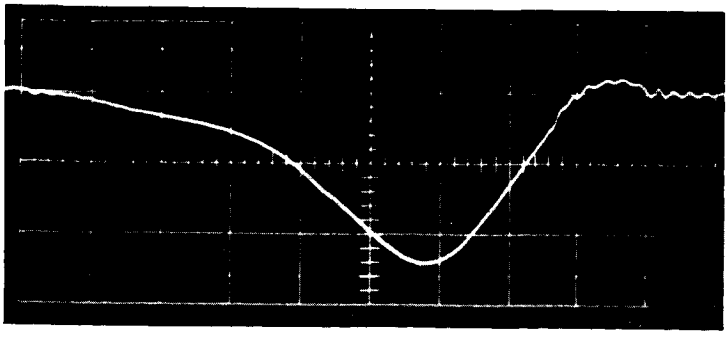
$I_i = 0.6$ amp

$uV_1 = 132$ mv $T_p = 1.16\ \mu$sec



$I_i = 1.2$ amp

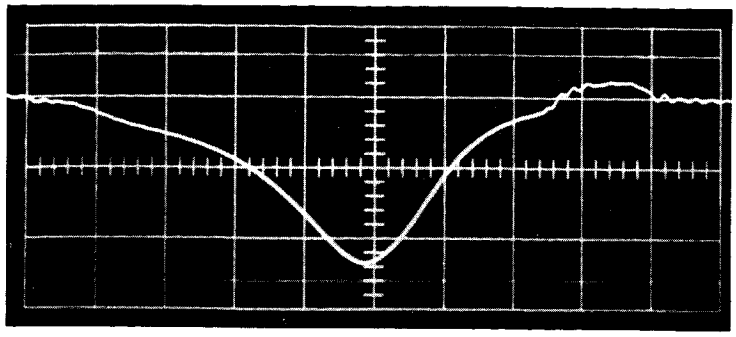
$uV_1 = 128$ mv $T_p = 1.18\ \mu$sec



$I_i = 8.0$ amp

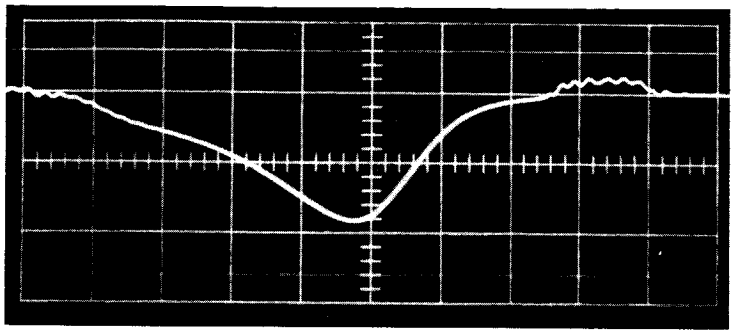
$uV_1 = 120$ mv $T_p = 1.18\ \mu$sec

FIGURE 3.16 CORE "C" I_R = Min Q I_W = Max Q T = 10° C T = 0.2 μsec/cm



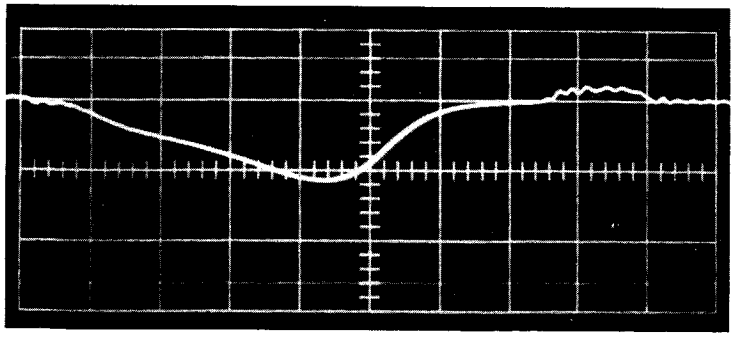
$I_i = 0$

$uV_1 = 119$ mv $T_p = 0.98$ μsec



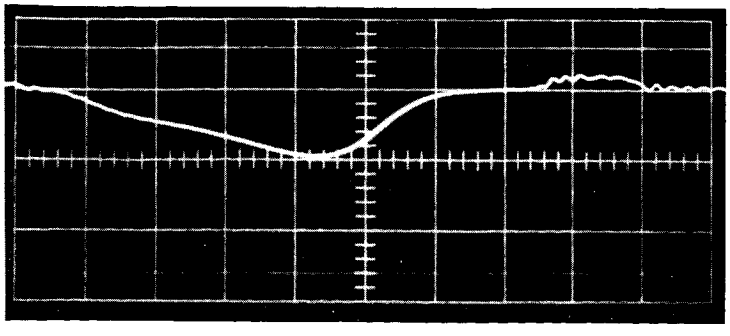
$I_i = 0.6$ amp

$uV_1 = 92$ mv $T_p = 0.95$ μsec



$I_i = 1.2$ amp

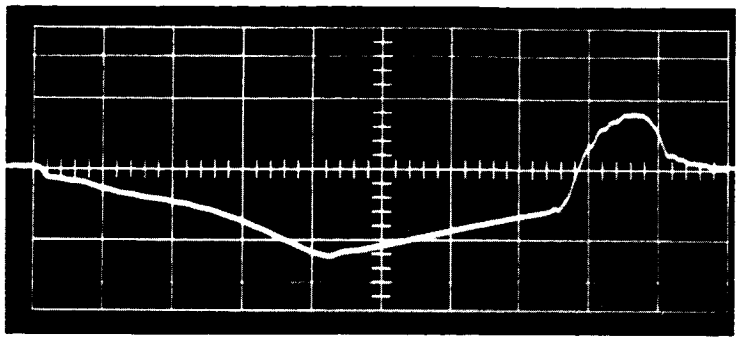
$uV_1 = 59$ mv $T_p = 0.88$ μsec



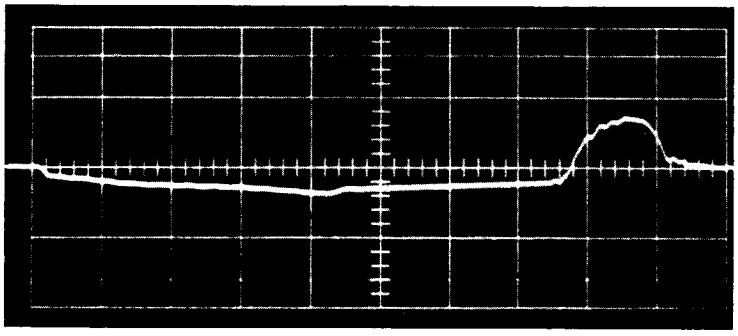
$I_i = 8.0$ amp

$uV_1 = 43$ mv $T_p = 0.88$ μsec

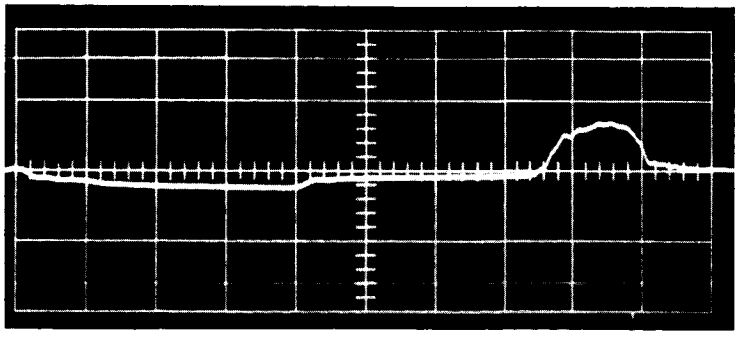
FIGURE 3.17 CORE "C" $I_R = I_W$ = Min Q T = 10° C T = 0.2 μsec/cm



$uV_1(1)$ = 27 mv



$uV_1(2)$ = 7 mv



$uV_1(3)$ = 4 mv

FIGURE 3.18 CORE "C" I_R = Min Q I_W = Max Q T = -10° C

4. INHIBIT CORE LOGIC PACKAGING STUDIES

The purpose of this study is the development of a packaging technique applicable to the logic memory portions of the proposed JPL Inhibit Core Logic System. The goals toward which this study is to be directed are:

1) Arrive at a final packaging configuration which will adequately meet the requirements of mechanical strength, environmental protection (including sterilization requirements), assembly technique, and verification.

2) Determine a set of materials which, when assembled in the recommended configuration, will yield a functional system that meets all requirements of compatibility and reliability.

3) Develop a manufacturing process incorporating fabrication by average electronic assembly personnel, provisions for assembly verification through in-process testing, quality control inspection, and adequate safeguards against normal hazards of assembly handling.

4) Provide a process flow chart and a set of detailed process specifications.

5) Provide criteria for optimum final wire routing and investigate methods for generating the final production wire lists using an IBM 7090 computing system.

4.1 JPL System Requirements

The final logic memory packaging configuration to be developed under this contract was subject to certain restrictions imposed by the JPL system for which it is designed. Along with these fixed requirements, a set of good practice standards must be established before actual design can begin. The most important factors which describe these two areas of concern are listed.

1) The basic form factor for the package is established by JPL drawing No. 430032, Typical Subassembly-14 inch, which describes a lightweight frame plug-in subassembly approximately 14 by 6 by 1 inch which has a web 0.10 inch thick running through the center.

2) The basic logic element is specified as a low-drive, coincident current ferrite core having an outside diameter of 0.080 inch, an inside diameter of 0.050 inch, and a thickness of 0.025 inch. (See Figure 4.1.)

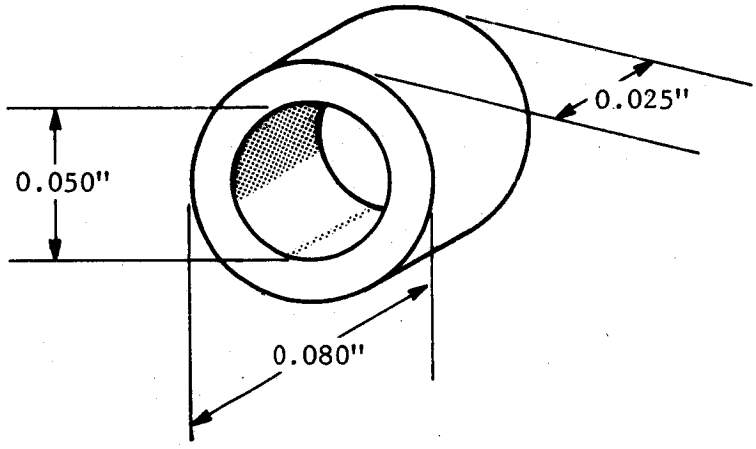


FIGURE 4.1 BASIC LOGIC ELEMENT

3) The wiring configuration is established by the logical equation list presented in JPL Technical Memo No. 341-32 Complete List of Logic Terms of the Magic and Corrections to Magic Logic Term List (TM No. 341-32) by David Rubin.

4) The environmental requirements are established in JPL Specification No. 30257 Environmental Specification Mariner B, Flight Equipment Type Approval Test Requirements (Assembly Level)

5) The reliability requirements should be established by JPL to adequately cover the applications for which the system is intended.

4.2 Design Standards

The following design standards will be maintained:

1) Ease of manufacturing should be accomplished by the use of well-known materials and production techniques where possible.

2) The mechanical configuration should be designed to optimize the electrical properties of the system.

3) Environmental protection should be built-in, not only to withstand service conditions, but to minimize all requirements for special out-of-service handling techniques.

4) Module replacement should be afforded on as low a subassembly level as practical to save on the costs of system repair and spare parts stock.

5) Test features should be incorporated which allow ease of production verification and in-service troubleshooting.

6) Both size and weight should be minimized where practical.

The JPL imposed requirements were treated as inviolable throughout the entire investigation. In the discussion which follows covering the four areas of concern, mechanical configuration, packaging materials, productions process, and final wire routing, the restrictions imposed in each area by these fixed requirements is noted. The degree of achievement of the design standards is discussed also. A set of recommendations is presented at the end which covers the present systems and describes certain changes which might be contemplated to further increase packaging efficiency.

Inspection of Figure 4.2 shows that the volume efficiency of the 64-core module is very poor. The area of the board is determined by the periphery required by the input and output termination pads. The number of pads is, in turn, fixed by the logical equations. If a single read clock is used in the present system, 102 pads is more than adequate (see Table 4.12) to handle the logic. The required minimum module circuit board periphery is therefore established by the logic. The actual board dimensions were set by the requirement that the logic memory fit within the confines of the subassembly plug-in dictated by JPL. Since the number of required input-output pads increases slower than the number of cores per module, a great improvement in volume efficiency may be achieved by increasing the number of cores per module. The smallest volume that can be achieved for the logic memory will obviously be reached when all the cores are placed in a single module.

In view of the discussion presented in the previous paragraph it would seem logical to establish a maximum on the number of cores which may be placed in a single module. Unfortunately this has not been established as a number under the present study. Two factors must be established before a number is arrived at. The allowable cost of a throwaway package must be fixed and the winding efficiency of average assembly personnel must be established for the proposed system. Wiring efficiency is, in this case, the probability of misswiring a core, breaking a wire, or scraping off enough wire insulation to cause a short circuit. This probability will determine production line yield. Because of the highly abrasive nature of the ferrite core surfaces and the sharp die fins left at the inside edges of the core by the manufacturing process, it may not be possible to wire even a 64-core mat in the intricate manner prescribed by the logic without running the risk of a very high module rejection rate. Scrape and abrasion tests were run (see Appendices B and C) on various sizes of wire coated with a variety of insulation materials. (See Appendices H and I.) The results could not be correlated to the actual production situation but did establish insulation scrape and abrasion as a severe problem area. For this reason it was decided to restrict the number of cores per module in a ferrite core system to the near minimum of 64.

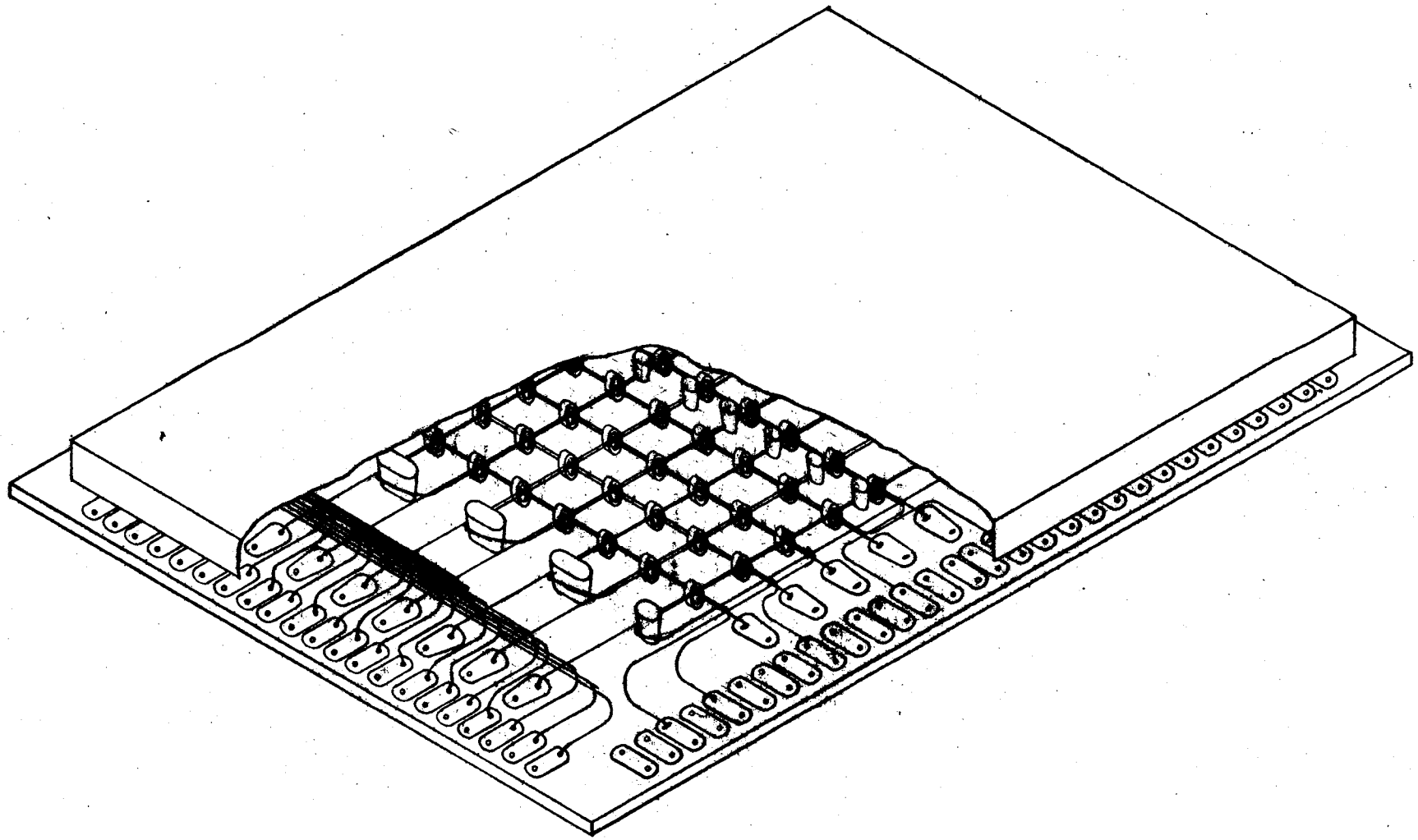


FIGURE 4.2 CUTAWAY PERSPECTIVE OF LOGIC MEMORY MODULE SHOWING CORE LAYOUT AND X/4 SELECTION WIRES

4.3 Packaging Configuration

4.3.1 Logic Module

The final logic module packaging configuration is shown pictorially in Figures 4.2 and 4.3. It may be described as a set of 64 cores stood on end in an eight-by-eight square array and held in position by the intersections of two orthogonal sets of eight parallel selection wires. The X and Y selection wire sets also hold the cores against the module printed circuit board in such a way as to restrict their motion normal to the board. All the cores are canted in the same direction which is approximately 45° to both the X and Y wires. The inhibit and clock wires are routed through the matrix as shown in Figure 4.12 allowing row-to-row transitions to occur only at the ends and center of the matrix. Stress relief pins are mounted at the center and ends of each row to act as a framework for routing the wires. The input and output termination pads are mounted around the periphery of the board and the test selection pads inside. The fully wired core mat is conformally coated and a hard epoxy coat is applied to give complete protection.

The package will be divided into each of its constituent parts and examined in detail. The thought processes which combined the system requirements with the design standards to arrive at the final package will be discussed as completely and accurately as possible. Test results which influenced the decisions appear in Appendices H and I will be referenced as required.

The number of cores per module was established at 64 primarily on the basis of the limitations involved in the wiring process and the requirements of the logical equations. The absolute minimum number of cores which must be accommodated by a single logic module is 60, set by the size of the gating structure required by the F4 flip-flop. A further analysis of the logic discloses that the whole logic memory of 478 cores can be mechanized in eight modules of 64 cores each. This establishes the maximum number of modules into which the logic memory may be effectively divided. Since module repair is felt to be impossible after encapsulation, the eight-module division establishes the minimum cost per module in a throwaway repair situation.

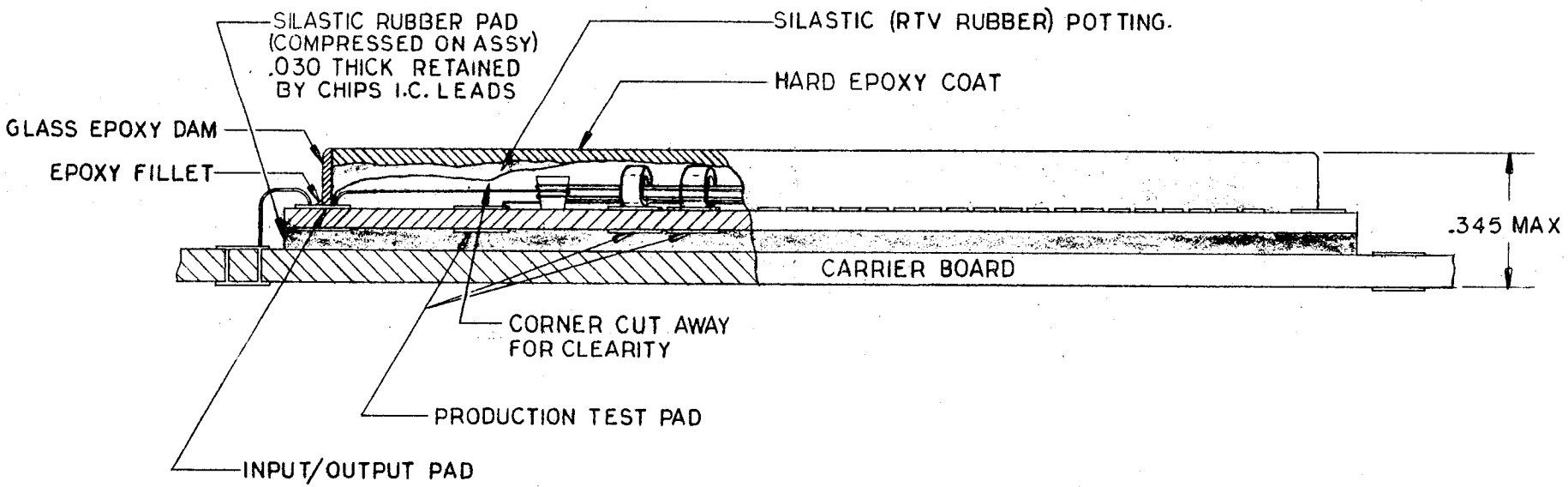


FIGURE 4.3 CUTAWAY PROFILE VIEW OF LOGIC MEMORY MODULE MOUNTED ON CARRIER BOARD

It was decided to stand the cores on end rather than lay them flat over holes in the board because of the registration problems associated with wiring on both sides of the board. Twice as many holes as cores must be drilled in the board to allow the wires to thread the cores in the manner prescribed by the logic. This would in turn require more board area to be used per core than in the upright configuration. Another serious problem encountered in the flat layout is associated with keeping the core threading window open after a significant number of wires have passed through it. The fact that some of the cores have as many as 17 wires to accommodate, would so restrict the winding procedure that considerably more than a minimum amount of wire would be required for each term. It could also be seen that the scrape and abrasion problems were in no way alleviated by this configuration. The upright core configuration was therefore adopted. Figures 4.4 and 4.5 show a partially wired and a fully wired core module. The fully wired module represents the F4 flip-flop for a single read clock system. The wire used for the X and Y lines is AWG No. 30 copper annealed with heavy formvar insulation. The logic wires are AWG No. 36 copper annealed with heavy formvar insulation. The fully wired board has never been checked out since it was constructed to prove process (rather than electrical) requirements.

The sense line which is threaded orthogonal to the inhibit and clock lines can most easily be wound for zero flux window area if an even number of columns is used for each matrix. A square array was chosen because it not only has an even number of columns but also because it tends to minimize the length and inductance per unit length of wires threaded through a memory plane. Under the set of wiring rules established by the production process, neither of these reasons is quite as valid as was originally anticipated when direct core-to-core wiring was allowed. The square array does, however, tend to decrease the amount of X/Y selection hardware required by the production test equipment.

The necessity of an individual core selection system required for the in-process wiring verification tester and the necessity of holding the core in a relatively fixed position during the wiring process dictated the use of X/Y selection grid wires. There wires need be available only during the assembly process and can therefore be terminated at pads located inside the peripheral input/output pads. These test pads can be plated on the bottom of the boards so that the production

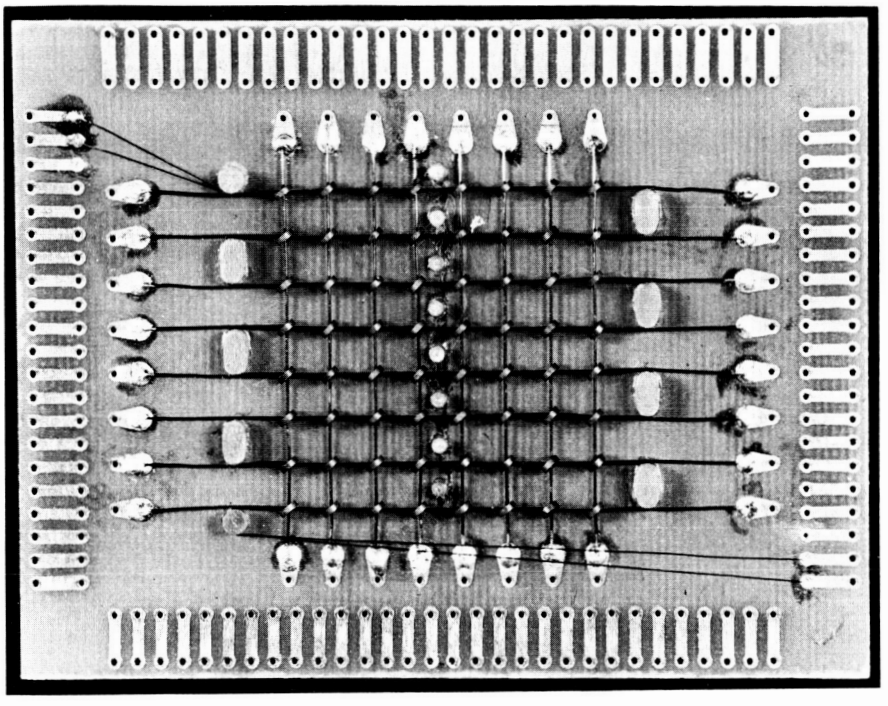


FIGURE 4.4 PARTIALLY WIRED CORE MODULE

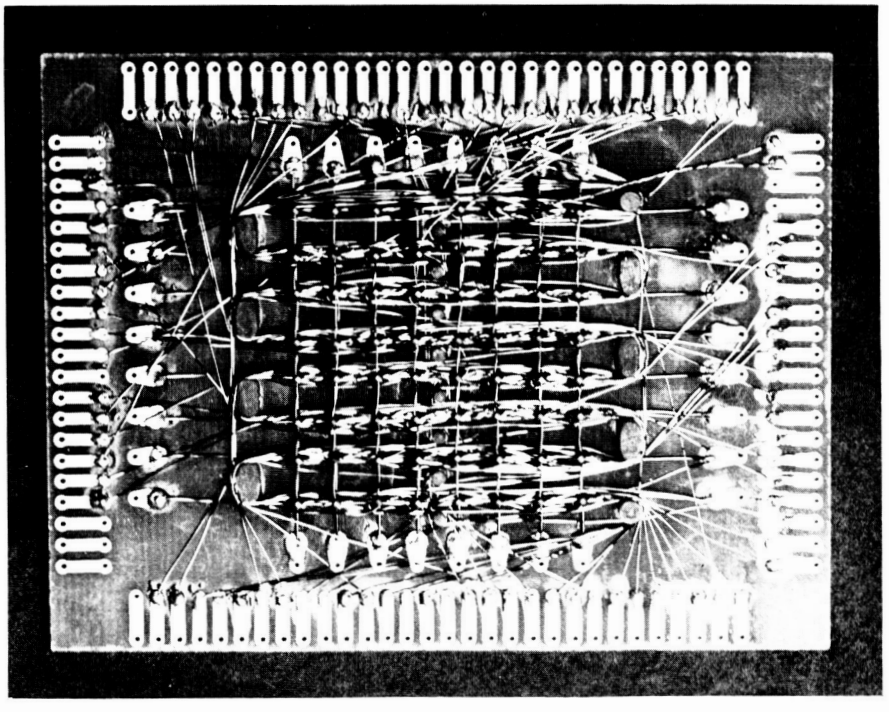


FIGURE 4.5 FULLY WIRED CORE MODULE

tester can be built into the assembly fixture without the selection wires interfering with the wiring process.

The stress relief pins were added to the module as a framework around which to wire the clock and inhibit lines. The necessity of having such a framework was discovered when an attempt was made to core-to-core wind the F_4 matrix. It was found to be almost impossible to keep the core threading window open without some framework for tying each wire into place. It was also felt that these pins would tend to keep the wires from further abrading the cores of one row after that row has been threaded. The pins, as shown, represent somewhat of a hazard in that they tend to bring many of the wires into very close proximity thereby increasing the probability of failure through short circuit. Other methods of supplying the required features should be investigated.

The input/output termination pad configuration is a direct application of well-established, state-of-the-art design practice. The pads are required to be only on one side of the board; however, if both sides of the board are identically etched, the number of photo-etched masks required is reduced by one. Through a study of the logic lists, the minimum number of pads required was set at 102. The mechanization of the P time clock could affect this considerably. It may also be stated that the module-to-module wire could be considerably simplified if a pair of pads were made available on each module for every active wire which threads the logic memory. Since there may be up to 80 such wires, the memory volume would increase considerably unless more cores were placed in each module. A drawing of the module circuit board for the proposed 64-core 102 input/output pad logic memory plane detailing the dimensions and positions of the circuit pads and stress relief pins is shown in Figure 4.6.

The decision to use an RTV conformal matrix coating under a hard epoxy shell was dictated by the environmental conditions in which the system is to be used. Because of the severe scrape and abrasion hazard of the ferrite wire insulation system, protection must be provided against the severe shock and vibration conditions required by the system specification. Movement of the cores relative to the wires must therefore be restricted as much as possible. Hard potting the entire matrix would undoubtedly accomplish this end; however, due to the

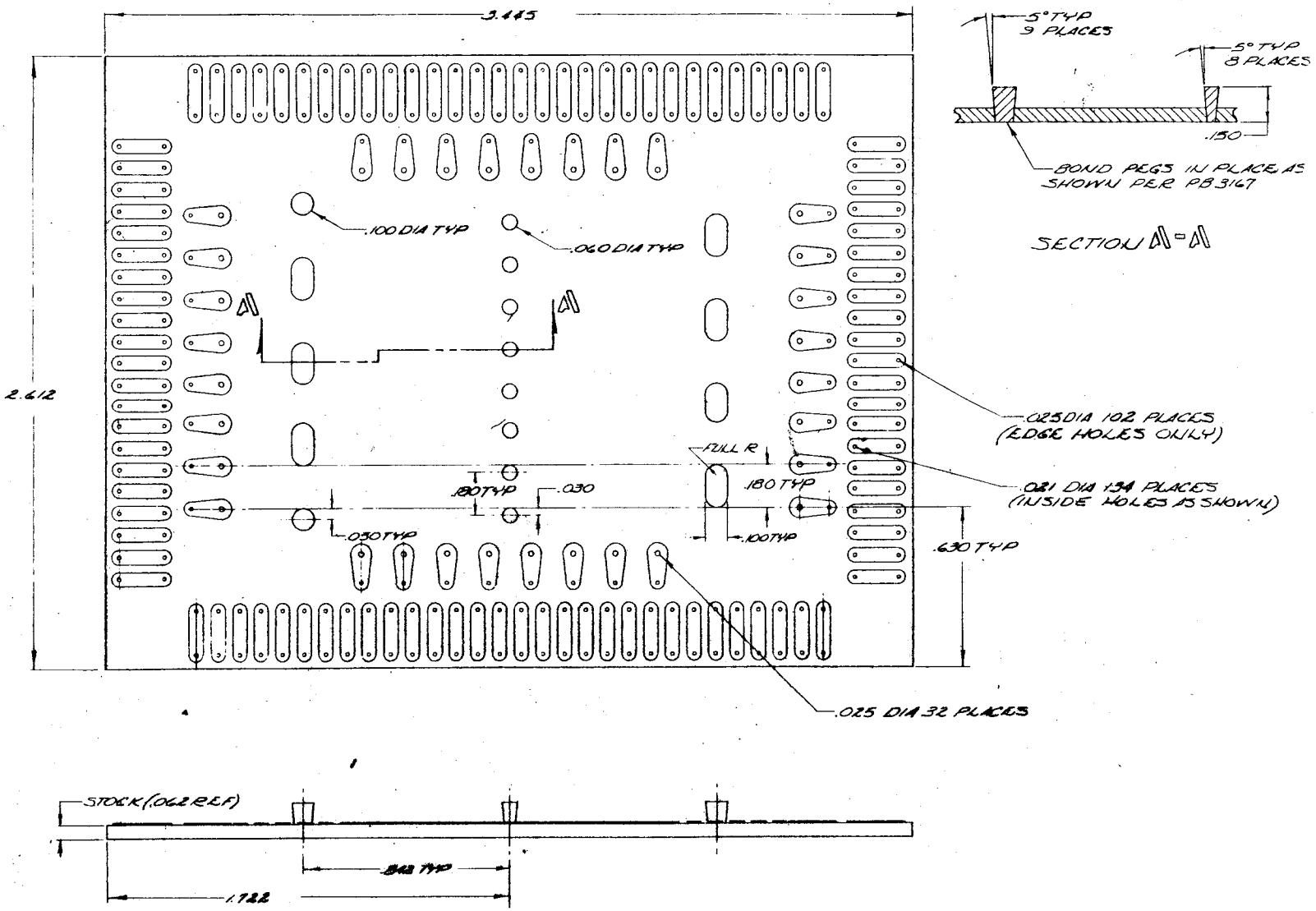


FIGURE 4.6 CONE MODULE CIRCUIT BOARD, DETAIL DRAWING

magnetostrictive characteristics of the ferrite material, the internal pressure generated by such a system would undoubtedbly seriously affect the electrical characteristics of the core. This fact is corroborated by test results reported in Appendix I. The same test shows that a least two RTV conformal coating materials have no effect upon the core switching characteristics. The decision to use a silastic conformal coating over the core-mat is based upon its mechanical damping characteristics and compatibility with the ferrite core material. The hard epoxy sheet over the conformal coat serves a number of extremely vital functions. It adds considerable rigidity to the module board, provides an extra measure of protection to the module during handling operations, and protects the conformal coating material from the corrosive sterilization atmosphere.

4.3.2 Logic Memory

For the purpose of this study the form factor of the logic memory was considered to be restricted to the subassembly plug-in described in JPL drawing No. 4300302, Typical Subassembly-14 inch as shown in Figures 4.7 and 4.8, the eight modules and their interconnections will fit into the JPL plug-in. A carrier board which is cut to fit against the center web of the plug-in is used to hold four modules and their interconnections. The modules are cemented to the carrier board with a thin silastic pad between the module circuit board and the carrier board. This is shown in detail in Figure 4.3. A silastic pad is also placed between the carrier board and the plug-in web to which it is fastened.

The module-to-module connections can be made by point-to-point wiring through a cable harness or by landing the interconnections on the carrier board and connecting the module pads to the carrier board pads with soldered-in leads. If the carrier board is to be used to form the interconnection pads, some thought must be given to assigning functional order to the module pads. From an analysis of one possible module layout presented in Table 4.6, it can be seen that at least 24 of the active wires which thread the logic memory are required by every module. By assigning certain functions to the unused pins of less crowded modules, the number of terms common to every module may be raised to 33 without requiring any modification of the basic 102-pad configuration. This allows the two 30-pad

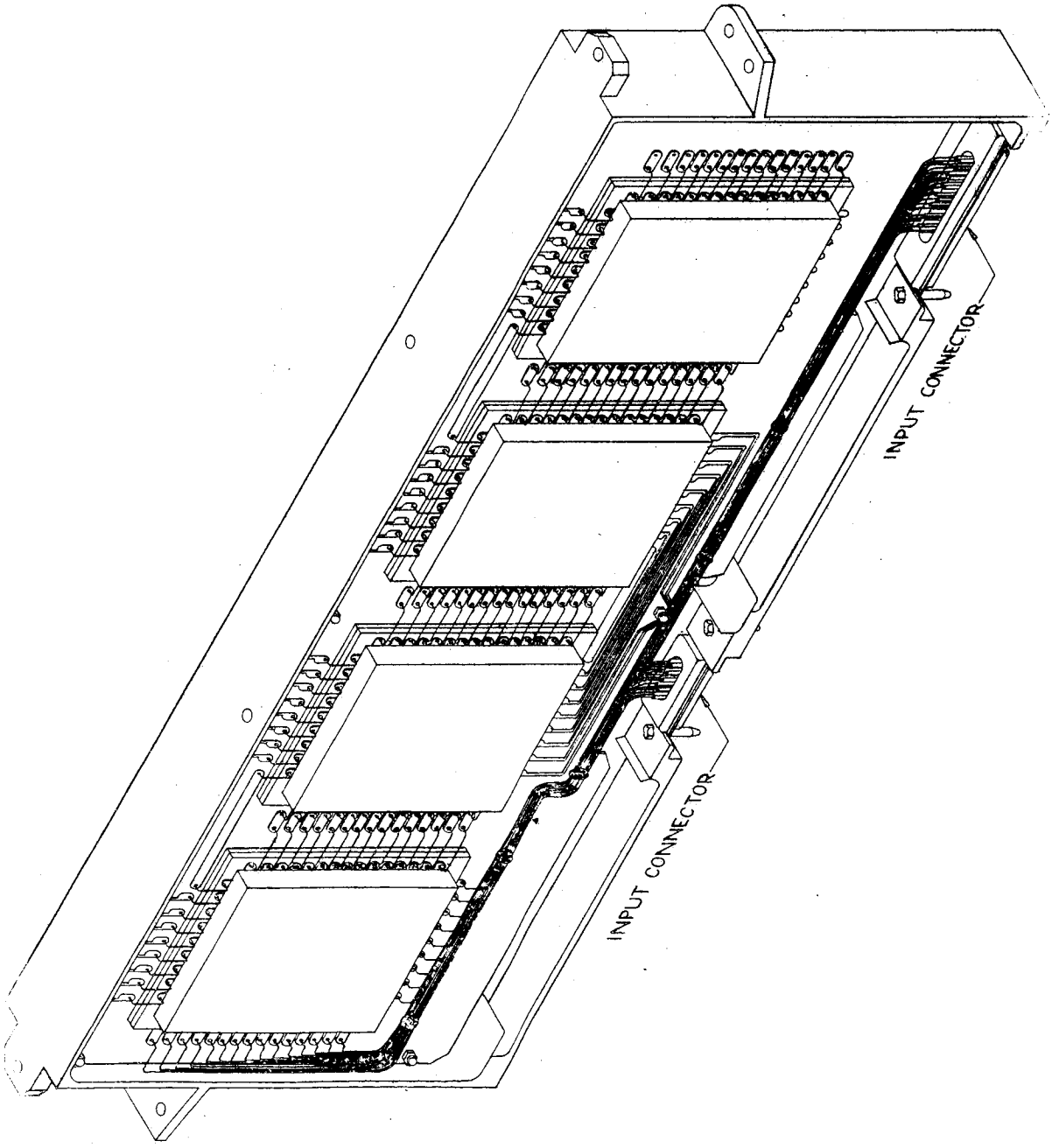


FIGURE 4.7 LOGIC MEMORY PROPOSED FOR USE IN THE JPL INHIBIT CORE LOGIC SYSTEM; ISOMETRIC VIEW

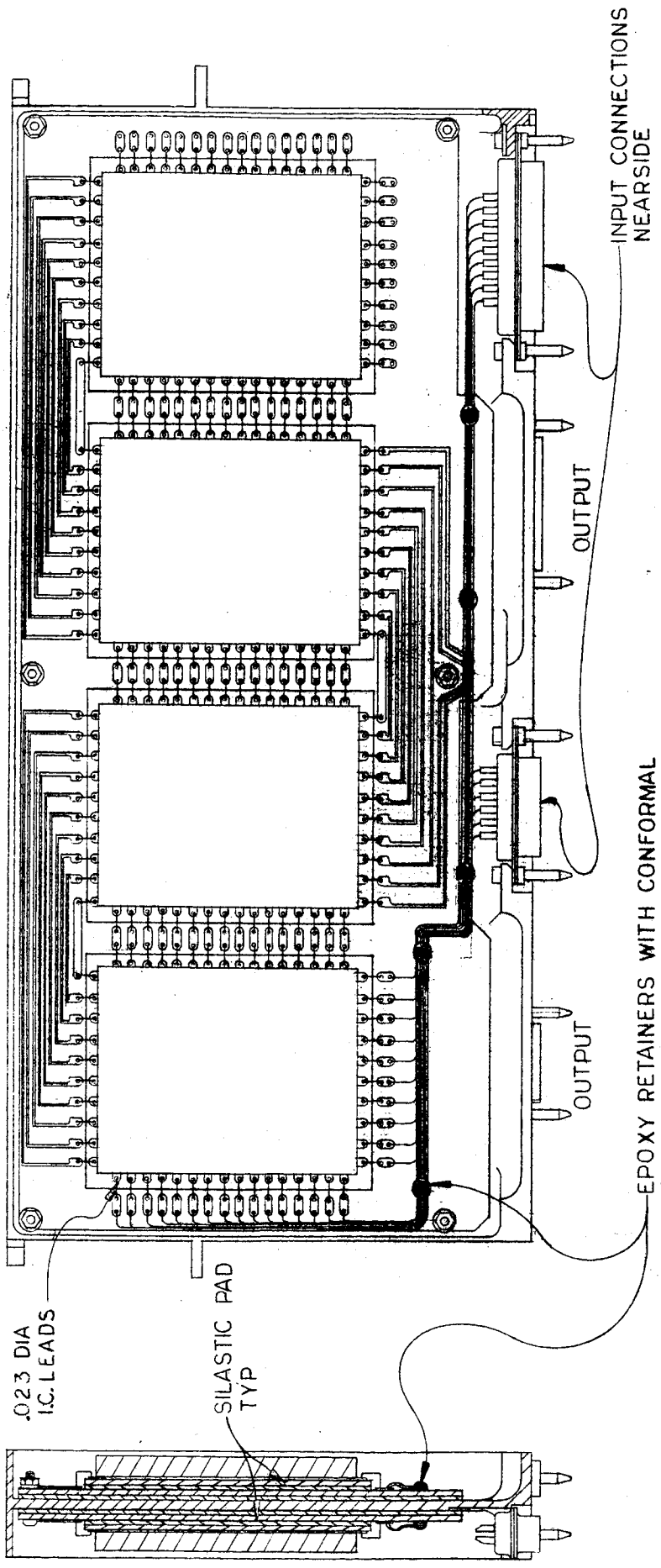


FIGURE 4.9 DETAIL OF LOGIC MEMORY LAYOUT

sides of the module to be labeled in terms of wire function without regard to the actual logic function of the modules. Since the 30 pad sides of the module are adjacent to one another in the proposed package configuration, they may be assigned and therefore wired straight across the board. Three of the remaining 21 pairs of pads may be treated in a similar manner. Four pairs of pads are required for the sense lines. Only 13 pairs of pads remain to be oriented according to the carrier board layout. This final step was not investigated because of the lack of time and the trivial nature of the problem.

Figures 4.7 and 4.8 do not show the total number of pads per module required to mechanize the logic but do demonstrate the feasibility of the recommended plan. The wiring of the sense lines is not shown in either of the illustrations. The sense lines are taken off adjacent module pads as twisted pairs and brought directly to the plug-in assembly output connector. The sense line should be kept as far away from the read clock line as possible.

4.4 Materials Selection

4.4.1 Wire - Size and Material

The functions performed by the wires used within the module fall into two categories. The first category covers all the wires which are required to make a module perform according to the logical equations. Specifically, they are the clock, inhibit, and sense wires. Wire size is dependent upon the electrical requirements of the memory and the maximum number of wires which must be threaded through a single core. The second category covers the X and Y selection wires which must thread each core for the production verification tests and must be rigid enough to hold the cores in place during the threading process.

The X and Y selection wires should be as small in diameter as possible since they pass orthogonally through a core and may therefore cover a considerable area of the core threading window. They must also be insulated from one another so as to keep their selection capabilities intact. Various types of wires were investigated; however, the insulation requirement disqualified all but standard

copper annealed magnet wire. Because of the poor mechanical properties of this material, AWG No. 30 was found to be the smallest size suitable for use in the matrix layout. Further investigation into this problem may reveal an insulating technique or a source of supply which would permit the use of some other material such as copper beryllium for the selection wires. Reducing the size of these wires would enhance the threading process considerably.

The active memory wires should be of as low a resistance as possible in order to minimize the memory line drive voltage requirements. The wires should therefore have the largest cross sectional area that is compatible with the wiring configuration. For the JPL specified current pulse program it was determined that for copper wire any size below No. 42 could be used without fear of exceeding the fusing level. Studies showed that AWG No. 38 copper annealed magnet wire is the optimum wire size and material for this application. Figure 4.6 shows a module threaded with No. 36 wire. Winding this plane was considered to be an unreasonable task for normal assembly personnel. The sense line requirements were not considered to be critical. It was therefore decided to use AWG No. 38 magnet wire for all the lines within the module except those required for production test selection.

The logic memory wires required to connect modules to the carrier board, active wires to the rest of the system, and module sense lines to the sense amplifier inputs must also be specified. The recommendations covering these areas are derived from Nortronics experience in module interconnection systems. The results of the wire material and size study are summarized in Table 4.1.

4.4.2 Wire Insulation

Selecting an insulating material for the wires which are required to thread the logic cores presented one of the most serious problems encountered in the entire packaging study. The requirements of high abrasion and scrape resistance dictated by the surface and edge characteristics of the ferrite core and ease of insulation removal dictated by the size and number of wires involved were found in almost every case to be directly opposed to one another. Those insulation

types which showed good resistance to damage under the core threading environment were found to be very difficult to strip by normal production line techniques. It was felt that, under the limited time allotted to the study, a conservative approach was required to insure the achievement of usable results. Scrape and abrasion characteristics were, therefore, given priority over stripping properties in arriving at the final recommendation.

Cores from several manufacturers were microscopically examined to determine the properties of their surfaces which might lead to insulation breakdown during the matrix threading process. While considerable variations in surface characteristics were discovered between ferrite cores manufactured for different applications, the surfaces of all the low drive, 80 mil, coincident current cores regardless of manufacturer displayed approximately those characteristics seen in Figures 4.9 and 4.10. The surface characteristics are fairly uniform and have a grain structure which approximates that of 400A silicon carbide paper.

The edges of the core, however, display a very nonuniform finish consisting of jagged protrusious and voids. Many of the cores were observed to have chipped areas both on the surfaces and along the edges.

A series of tests were developed for the purpose of rating wire insulations in terms of their resistance to the abrasion and scrape mechanisms to be found in the core wiring process. The test procedures are described in Appendix H and the test results are presented in Appendix G. An initial screening process of all the types of film insulating materials available narrowed the field to the four listed in Table 4.1.

TABLE 4.1 INSULATING MATERIALS CONSIDERED FOR INTERNAL MODULE WIRES

Trade Name	Abbreviation	Manufacturer	Chemical Family
Formvar	HF	Anaconda	Vinyl acetate resin
ML Polymer	ML	Anaconda	DuPont high temperature resin
Polythermaleze	PTE	Anaconda	Polyurethane resin
Solvar		R.E.A. Magnet Wire Co.	Polyurethane resin

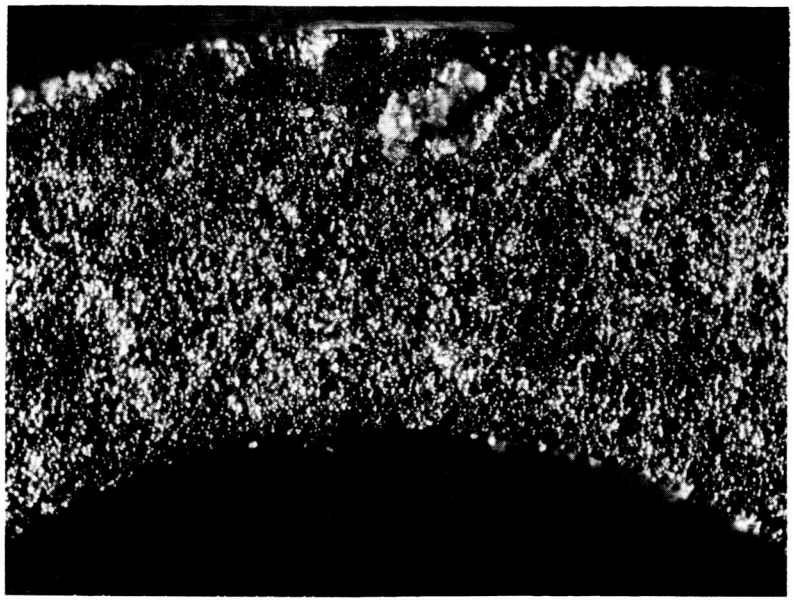


FIGURE 4.9 EMI 81-104 FERRITE CORE (SECTION 100X)

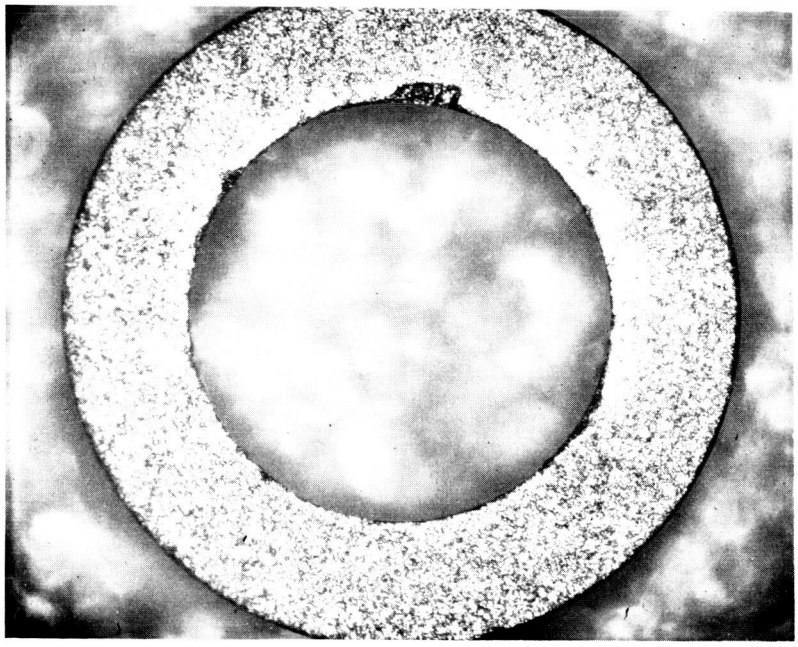


FIGURE 4.10 AMPEX 802-40 FERRITE CORE (50X)

The Formvar coated wire was observed to have by far the highest resistance to scrape of any of the wires tested. The ML coating on the other hand was observed to be superior in the abrasion test. The Polythermaleze coated wire performed relatively poorly in both situations and the solvar wire performed so badly in all tests that it was not included in the test results. On the basis of the core lay-out established by the package configuration, it was determined that the scrape test represented a better analogy to the actual assembly situation than did the abrasion test. The insulation materials were therefore rated in the order shown in Table 4.1. This result was used to narrow the field to the Heavy Formvar (HF) and ML insulation. Triple Formvar (TF) may be used to reduce abrasion resistance if required.

Ease of insulation removal was established as the criterion upon which to base the final choice. A second series of tests were set up to establish a rating system to cover this area. The following criteria were used to determine the quality and ease of the stripping processes investigated; the stripped wire must exhibit good solderability, freedom from corrosive chemicals, and no reduction of cross-section. The process must provide freedom from health hazards, adequate protection for the assembly, ease of inspection, low process time, and adequate compatibility with the rest of the assembly process. The tests are described in Appendix H, and the results presented in Appendix I.

The only process which effectively met most of the criteria mentioned in the previous paragraph was chemical stripping followed by chemical neutralizing and ultrasonic cleaning. Only the Formvar was found to be compatible with this involved process. The ML insulation was thus disqualified.

Further investigation should be made into this area. The stripping process required by Formvar is involved and requires special handling and materials. The PTE and Solvar insulations were originally included because both are relatively easily stripped in a molten solder bath. However, the results of the investigation to date clearly point to the use of Formvar as the insulating material for the wires to be routed through the core mats.

Teflon insulation is recommended for the module-to-module and module-to-system wire cables. The results of the studies conducted on wire material, size, and insulation are summarized in Table 4.2.

TABLE 4.2

Function	Insulation Material	Wire Size AWG	Wire Description
Internal Module Wires			
Clock lines	Heavy-Formvar	No. 38	Solid annealed copper
Inhibit lines	Heavy-Formvar	No. 38	Solid annealed copper
Sense lines	Heavy-Formvar	No. 38	Solid annealed copper
X/Y Selection lines	Heavy-Formvar	No. 30	Solid annealed copper
Memory System Wires			
Module to Carrier Board	None	No. 26	Solid copper beryllium
Active line cables	Teflon	No. 26	Stranded annealed copper
Sense line cables	Teflon	No. 26	Stranded annealed copper twisted pair.

4.4.3 Memory Core Coatings

Because of the severity of the effects of the core surface and edges on the matrix wire insulation, it was felt that an investigation into the benefits of film coating materials on the scrape and abrasion characteristics of ferrite cores was justified. The investigation was only carried to the point at which it was established that core coatings could provide a considerable improvement in these areas. Tests were performed on both Formvar and Solvar insulation materials which compared the insulation damage arising from cores spray coated with Krylon to that arising from uncoated cores. An 87% improvement in cut-through resistance was observed for both insulating materials for the limited sample tested. This would indicate that a significant increase in winding efficiency could be realized through the use of a suitable core coating. The test procedure is given in Appendix H and the results in Appendix I.

If a core coating is to be introduced effectively into the system, a suitable application process must be developed. The present study was not able to carry the investigation further. However, for future reference, the materials which might be investigated for this purpose are Polyurethane, Epoxy, Teflon, Kel-F, and Solid Film Lubricant.

4.4.4 Embedment

Logic module embedment is felt to be required for matrix protection against both the hazards encountered in normal handling and the specified operating shock and vibration environment. An analysis of internal stresses created by a normal hard epoxy embedment of the core-wire system is given in Appendix I and indicates that under the present JPL environmental requirements pressures as high as 12,000 psi, may be applied directly to the core. That this excessive pressure is sufficient to destroy the electrical properties of the core is demonstrated in the embedment tests which are presented in Appendices H and I. The application of a conformal coating directly over the core matrix to protect it from the shrinkage stresses created by the epoxy is clearly needed. The embedment stress analysis demonstrates the drastic pressure reduction which may be achieved by this solution. The embedment tests also indicate that the cores suffer no measurable damage when a conformal coating is placed between the hard epoxy overcoat and the cores.

The requirements of the conformal coating material are that it be compatible with the wire insulation, circuit board, core material, and epoxy overcoat over the temperature environment specified for the system. Two such materials were found which had the characteristics required and could provide protection for the core. Both General Electric's RTV 11 and Dow Corning Sylgard 182, while offering the right combination of mechanical and chemical qualities for the system under normal operating conditions, suffer severe corrosive damage under the effects of the Freon 12 atmosphere which is used for system sterilization. The conformal coating must, therefore, be completely protected from the atmosphere by an inert shell. Both materials are satisfactory if properly applied and cured. The Sylgard 182,

however, is more drastically affected by contamination and tends to be somewhat unstable in a high shock environment. For these reasons RTV 11 is recommended for use in the final package.

The material recommended for the module shell in Scotchcast 241, a semi-rigid epoxy known for low stress buildup under temperature variation, excellent thermal shock resistance, and compatibility to the other material elements of the system. The characteristics of the conformal coating and outer shell materials are summarized in Table 4.3.

TABLE 4.3 CONFORMAL COATING AND OUTER SHELL CHARACTERISTICS

Function	Trade Name	Manufacturer	Characteristics
Conformal Coat	RTV 11	General Electric	Soft Silicone Rubber, Opaque, excellent stress relieving properties, attacked by Freon 12
Outer Shell	Scotchcast 241	Minnesota Mining & Manufacturing	Epoxy anhydride, semi-rigid, brown, heat-cured, excellent thermal shock resistance, low internal stress buildup due to temperature variation, negligible outgassing.

4.4.5 Wire Termination

Three methods of wire termination were investigated:

1) Thermal compression bonding
2) Resistance welding

3) Soldering

Soldering was the only method which proved to be useful throughout the memory. Standard hand soldering techniques are therefore recommended for all memory electrical connections. The material to be used for internal module board connections is Sn 50 high temperature solder. For external module connections it is recommended that Sn 63 low temperature solder be used and that soldering iron temperature be controlled during this process so that internal module connections will not be disturbed during the module interconnection process. Soldering techniques are discussed in the Appendices H and I.

4.4.6 Circuit Boards

Epoxy glass laminate is recommended as module circuit board material, having been established as an industry standard for printed circuit use.

4.4.7 Stress Relief Pins

The stress relief pins should be made of a material which will insure properties of high resistance and high strength such as nylon.

4.5 Production Process Description for Logic Memory Module Assembly

The module assembly flow chart shown in Figure 4.11 has been established to show the sequence of steps required to construct a typical logic memory module. The process documents which describe the steps to be followed are presented in Appendix G. The following discussion is presented to clarify the flow chart and to cover details which are not included in the process specifications.

The four basic components from which the logic modules are constructed must be bought in to specification and stocked before the actual assembly process can begin. The flow chart, therefore, starts at the buy-in level and indicates circuit boards, logic cores, wire, and embedment material supplies. The

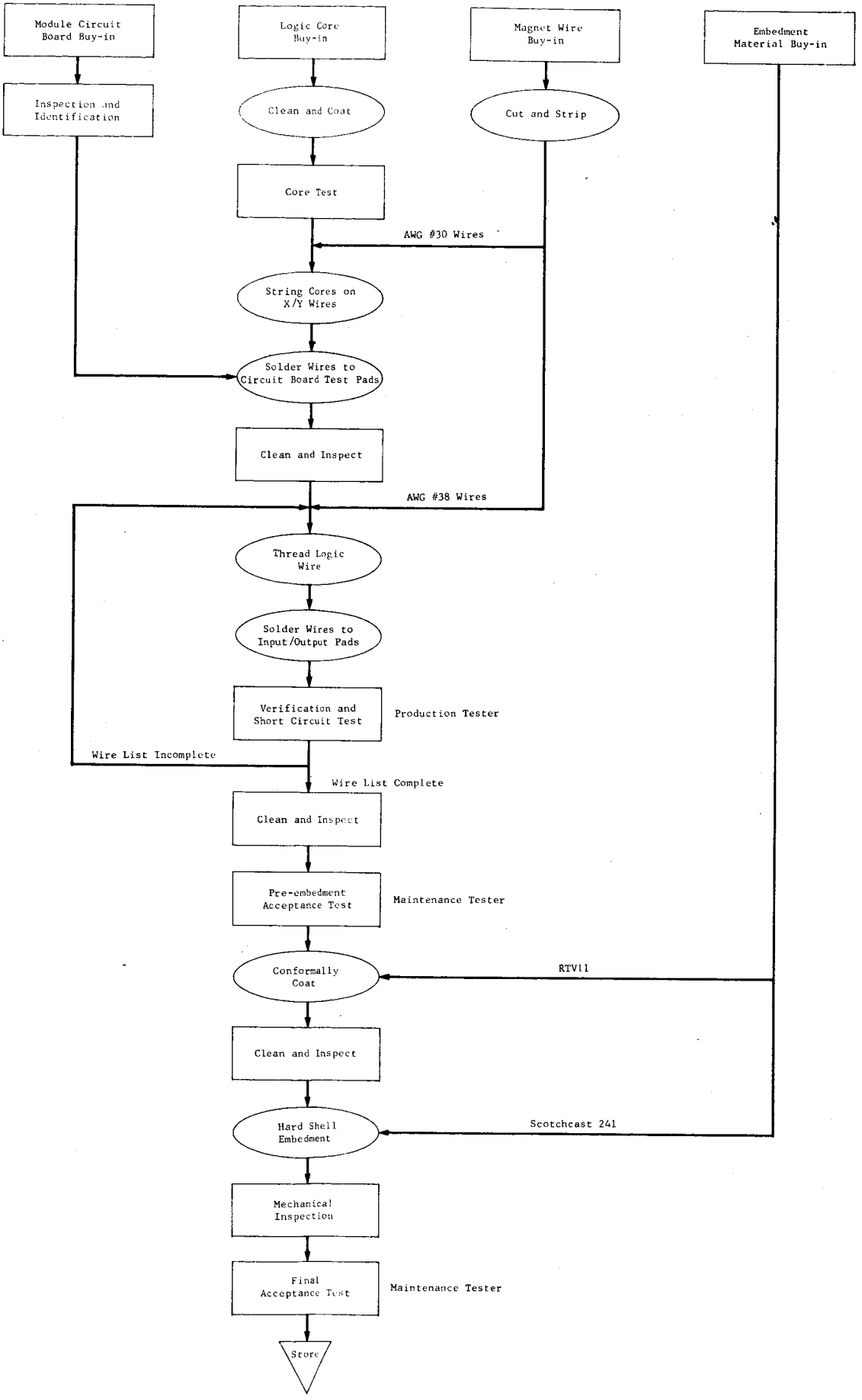


FIGURE 4.11 LOGIC MODULE ASSEMBLY FLOW CHART

circuit boards are inspected and identified according to function, the logic cores are cleaned, coated, and tested to the purchase specifications to isolate those damaged in handling. The wires are cut to length as specified on the wiring lists, stripped of insulation, and identified. The process specification for these steps are presented in Appendix G with the exception of the core coating process, for which a suitable coating has not been established.

During the second level of process steps the cores are mounted on the module circuit board and held in position by the X/Y production test selection wires. This is accomplished by stringing eight cores on each of the eight X lines, and soldering the X lines to the proper pair of test pads. The Y lines are routed such that each line threads one core out of each of the eight groups connected by the X lines. The Y lines are then soldered to the respective test pads. The X and Y lines are pulled taut so that they form a supporting grid for the 64 cores which are fixed at the intersections of the wires.

The third level is the most complex portion of the assembly process. The clock, inhibit and sense wires, referred to hereafter as logic wires, are threaded through the matrix. Because of difficulty of identifying wires within the matrix after a few have been threaded, and the impossibility of removing a wire after several wires have been threaded on top of it, the recommendation is made that this process proceed a wire at a time with a 100% electrical verification test made after each wire is threaded. A piece of test equipment designed for this purpose is described in Section 5. The tester may be wired directly into the assembly fixture since it must only connect to the test pads which are located on the under side of the circuit board. A probe may be used to connect the logic wire terminals to the tester. A test to determine wire-to-wire short circuits should also be made at this time.

Although 100% verification is provided by the production tester, the wire threading process is a demanding and tedious task at best. Any production aids which can be provided to make the task easier should be seriously considered. A visual display which could project the work piece onto a properly registered screen so that the wire route is shown superimposed upon the matrix board may prove to be of great benefit. The work piece projection could be accomplished

optically at a reasonable price. A series of screens could be provided, each of which contains a single wire route and other information pertinent to the process. The screens could directly represent wiring charts produced by the computing system used to generate the final wiring lists. A second projector could be used to provide a mark which would show the assembler her present position along the route and in which direction she must proceed. All details have not been worked out for a system such as this; however, there seem to be no problems at present which could not be overcome.

After the last logic wire has been threaded and soldered in position the board should be carefully inspected and cleaned in preparation for the application of the conformal coat. A pre-embedment acceptance test should be performed to insure that no short circuits or broken wires have been provoked during the handling processes. If a single short circuit is evidenced at this time, it is recommended that the module be rejected and destroyed. Repair may be possible; however, it is felt that the price paid in reliability assurance is not worth the gain. Repair of broken wires may be accomplished by stringing a new wire in place of the old, cutting the old wire away from the pads, and gluing the ends down away from other wires.

After a module has passed the pre-embedment acceptance test performed by the maintenance tester described in Section 5, the conformal coating is applied to the matrix. The coating must completely cover all wires and cores which lie within the area surrounded by the test pads. The proper curing schedule should be adhered to to insure that desired mechanical characteristics are built into the system.

Cleaning and inspecting are again required before the final hard shell epoxy embedment may be applied. No electrical tests are performed because the module is now considered to be unrepairable. After the outside shell has been applied and properly cured, a thorough mechanical inspection is performed and the module is cleaned to prepare it for final acceptance testing. The final acceptance test is performed again on the maintenance tester. A module rejected at this level is destroyed. The accepted modules are sent to the stockroom or the logic memory subassembly area.

The logic memory assembly process is not discussed in great detail in this report since all procedures required are standard production methods and are adequately covered by existing JPL process specifications.

4.6 Inhibit Core Logic Wire Routing

The final task to be performed before a complete set of module specifications can be itemized is that of determining the exact path to be followed by each logic wire within each module. Before this can be attempted it is necessary to assign the logic tasks to the individual cores as defined in the JPL logic lists. It is then necessary to establish a set of rules which will guide this task to a conclusion compatible with the design standards and fixed requirements under which this study is conducted. The wiring configurations which must be adhered to for both the active logic wires and the sense lines have been established in Paragraphs 3.2 and 4.2. These are illustrated in Figures 4.12 and 4.13. Any system optimization attempted during this phase of the design must, therefore, be accomplished by choosing a core task assignment which is best suited to the established wire routing rules. To accomplish this the wire routing rules must be specified in detail and a set of criteria for core task assignment determined.

Paragraph 4.6.5 of this report discusses the task of performing the core task assignment and wire routing operations using an IBM 7090 computing system. The feasibility of optimizing a point-to-point wiring system is discussed briefly, a flow chart is presented for programming the system under consideration, input-output format is discussed, and auxiliary uses for such a program are presented.

4.6.1 Detailed Rules for Threading Active Lines Through Module Matrix

A list of detailed rules for threading the active lines through the 8 x 8 module matrix is presented below:

1) The P time write clocks, which are used as inhibit terms, are threaded through the matrix rows in the sense shown in Figure 4.14. The cores in which these clocks are used as inhibit terms (logically shown as $\overline{P}_i$) are shown wired in the same direction as the normal wire route. The cores in which the P clock lines are used as write clocks (logically designated as P_1) are threaded in a direction opposite to the normal wire route. The current in these wires flows in the same direction as the arrows shown in Figure 4.12.

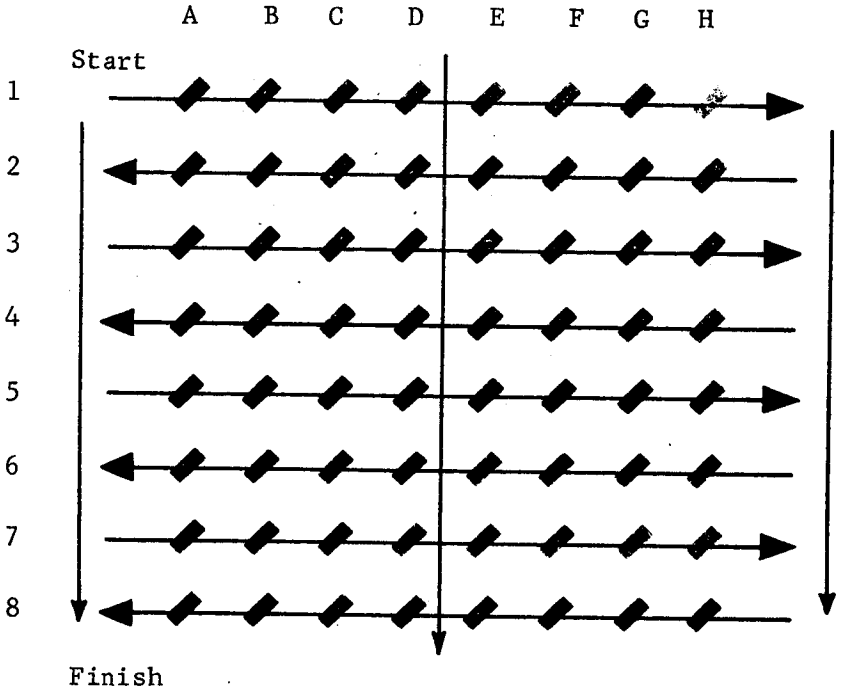


FIGURE 4.12

Illustration of the sense in which the active logic wires thread the module matrix. The wire which threads all the cores in the manner defined by the arrows is defined as the normal wire route. Row to row transitions are allowed only along the directions described by the vertical arrows.

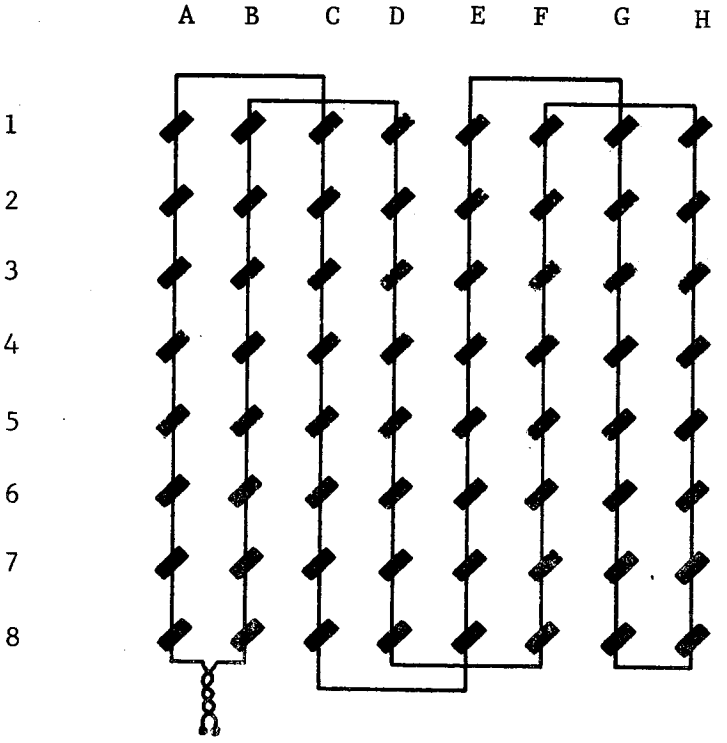


FIGURE 4.13

Illustration of sense line configuration recommended for minimum noise coupling and maximum shuttle cancellation.

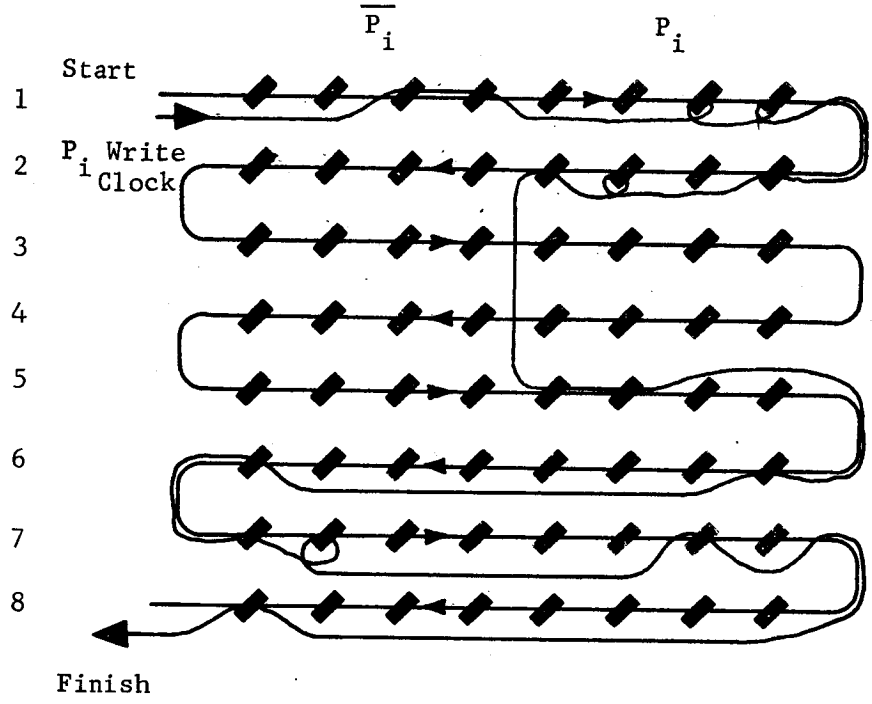


FIGURE 4.14

Shows an example of the threading of a P time write clock which is used both as a write clock and as an inhibit. The normal wire route is also shown with its start and finish points labeled.

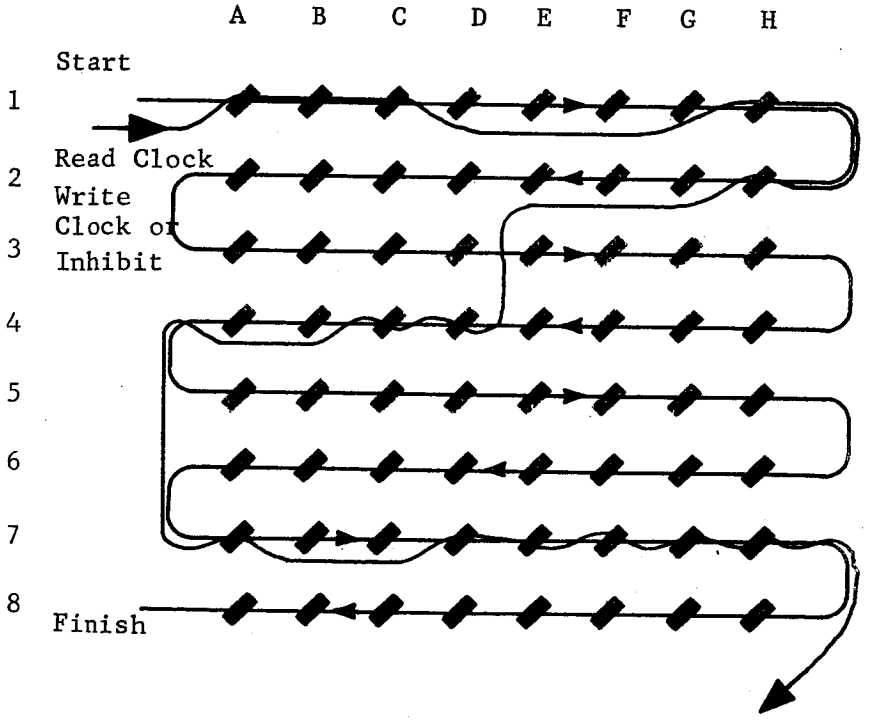


FIGURE 4.15

Shows an example of the threading of an inhibit, or the system write clock. All read clocks are threaded similarly but may not change rows in the middle of the matrix. The normal wire route is also shown.

2) The system write clock, the read clocks (system read clock and P time read clocks if used), and inhibit wires are threaded through the matrix in the direction illustrated in Figure 4.15. Current flows in the read clock and inhibit lines in the direction shown by the arrows. The system write clock line is the only active wire in the system which carries current in the opposite direction.

3) The sequence in which the active wires are threaded is as follows: read clocks, write clocks, inhibit lines.

4) The input pads are assigned as the top 30 and left side 21. Therefore, the threading process generally starts at the upper left-hand corner and proceeds row-by-row along the normal wire route to the lower left-hand corner.

5) The matrix may be entered at the left ends of rows 1, 3, 5, 7, at the right ends of rows 2, 4, 6, 8, or at the center of row 1. The matrix may be left at the left ends of rows 2, 4, 6, 8, at the right ends of rows 1, 3, 5, 7, or at the middle of row 8. Rows may be skipped entirely if the row contains no cores to be threaded.

6) Changing rows may be accomplished only at the center or ends of the matrix. When changing rows, wires should be bent around the stress relief pins provided.

4.6.2 Rules for Wiring Sense Lines

The rules to be followed during the sense line winding process are presented below. These rules are based upon the sense line discussion in Paragraph 3.2.

1) Where possible, the sense lines will be wound in the general configuration shown in Figure 4.13. This configuration must be followed closely, particularly in larger matrices.

2) The cores of the individual logic matrix will be kept in a tight grouping of 4 to 8 columns, where possible.

3) The sense lines will be wound last in order to maintain the zero flux window geometry inherent in the recommended sense line configuration.

4) The sense lines will be brought out of the matrices to the peripheral terminal pads as tightly twisted pairs. Twisted pairs should be used to connect the module outputs to the sense amplifier inputs.

4.6.3 Logic Matrix Assignments

The final wiring lists must be generated in accordance with the rules established in the previous discussion. The active line and sense line optimization criteria must be applied initially to the assignment of a logical task, to each of the cores within each memory module as dictated by the logic list. The first level of assignment is necessarily the laying out of the individual logic matrices within the allowed memory module structure and in conformance with the sense line wiring rules. It is probably not justifiable to program this operation on a computer in view of the limited number of matrices and the restrictions placed upon the allowable number of combinations of the matrices. The rules to be followed for logic matrix layout are:

1) The number of cores per module is restricted to 64.

2) The number of wire terminations per module should be minimized.

3) The number of common terms between adjacent modules should be maximized.

4) The average number of matrices per module should be minimized.

5) The maximum number of matrices per module should not deviate from the average more than is absolutely necessary.

Table 4.4 is a tabulation of the wires required to thread each of the logic matrices in addition to the number of cores required to mechanize each matrix. Table 4.5 shows a more detailed breakdown of the threading of the P time clock and inhibit terms. From these tables and a knowledge of the sense line wiring and matrix layout rules, a final matrix assignment can be made. The sense line

TABLE 4.4 FLIP-FLOP CORE AND WIRING TABULATION

Multi Bit Registers

	A		B		C		I		P		R		T	
	T	F	T	F	T	F	T	F	T	F	T	F	T	F
A	x	x	x								x	x		
B	x	x	x	x							x	x		
C					x				x				x	x
I			x		x	x	x	x						
P							x		x	x				
R			x								x	x		
T		x									x	x	x	x
F_1	x	x			x	x					x	x		
F_2	x	x	x											
F_3	x	x							x	x	x	x		
F_4	x	x	x	x			x	x	x	x		x	x	x
F_5	x	x	x	x	x	x			x	x	x	x	x	x
G														
J	x								x	x				
K_1	x	x	x				x	x	x	x	x	x	x	x
K_2	x	x	x				x	x			x	x		x
K_3	x	x		x			x	x	x	x	x	x	x	x
K_4	x	x	x	x			x	x	x	x	x	x	x	x
K_5	x	x	x	x			x	x	x	x	x	x	x	x
K_6	x	x	x	x			x	x	x	x	x	x	x	x
E	x	x	x	x	x	x	x	x	x	x	x	x	x	
M	x	x	x	x	x	x			x	x	x	x	x	x
N					x	x			x	x				
Sr					x	x			x					
Indep.	1													
$P_{inh.}$	1		2										2	
P_W	1		2						1		1		2	
P_R	1		2						1		1		2	
Mm	x	x	x		x	x	x							
C_W	x		x		x		x		x		x		x	
C_R	x		x		x		x		x		x		x	
Wires	40		32		19		22		32		35		30	
Cores	48		13		10		12		20		31		18	

TABLE 4.4 FLIP-FLOP CORE AND WIRING TABULATION (Continued)

Auxiliary Storage

	F_1		F_2		F_3		F_4		F_5		G		J	
	T	F	T	F	T	F	T	F	T	F	T	F	T	F
A	x	x	x	x	x		x	x	x	x				
B			x	x	x	x	x							
C	x		x		x		x	x						
I	x							x						
P					x		x							
R			x	x	x	x	x							
T	x	x			x	x	x	x	x					
F_1	x		x	x	x	x	x	x			x			
F_2			x	x	x	x		x						
F_3	x	x			x	x				x				
F_4	x	x	x		x	x	x	x	x	x				
F_5	x		x	x	x	x	x	x	x	x	x	x		
G									x	x	x	x	x	
J	x				x		x		x	x	x	x	x	
K_1	x	x	x	x	x	x	x	x	x	x				
K_2	x	x		x	x	x	x	x	x	x	x	x		
K_3	x	x	x	x	x	x	x	x	x	x				
K_4	x	x	x	x	x	x	x	x	x	x	x	x		
K_5	x	x	x	x	x	x	x	x	x	x				
K_6	x	x	x	x	x	x	x	x	x	x	x	x		
E	x	x	x	x	x	x	x	x	x	x	x	x		
M	x	x	x	x	x	x	x	x	x	x	x	x		
N	x	x												
Sr											x	x		
Indep.									1		1			
$P_{inh.}$	4		3		3		5		2		2		1	
P_W	4		3		4		4		2		2		1	
P_R	4		3		4		4		2		2		1	
Mm	x	x	x		x	x	x	x	x					
C_W	x		x		x		x		x		x		x	
C_R	x		x		x		x		x		x		x	
Wires	47		41		51		51		38		28		7	
Cores	39		29		32		60		29		12		2	

TABLE 4.4 FLIP-FLOP CORE AND WIRING TABULATION (Continued)

Operation Code Register

	K_1		K_2		K_3		K_4		K_5		K_6	
	T	F	T	F	T	F	T	F	T	F	T	F
A												
B												
C												
I												
P												
R												
T												
F_1												
F_2												
F_3	x	x			x	x	x	x	x	x	x	x
F_4	x	x	x	x	x	x	x	x	x	x	x	x
F_5												
G												
J												
K_1	x					x	x	x	x	x	x	x
K_2			x			x	x	x	x	x	x	x
K_3					x	x	x	x	x	x	x	x
K_4					x	x	x	x	x	x	x	x
K_5					x	x	x		x		x	
K_6					x	x	x		x		x	
E	x	x	x	x	x	x	x	x	x	x	x	x
M	x	x	x	x	x	x	x	x	x	x	x	x
N		x		x	x	x		x		x		x
Sr												
Indep.												
$P_{inh.}$	2		2		2		2		2		2	
P_W	2		2		2		2		2		2	
P_R	2		2		2		2		2		2	
Mm	x	x	x	x	x	x	x	x	x	x	x	x
C_W	x		x		x		x		x		x	
C_R	x		x		x		x		x		x	
Wires	20		18		30		29		29		29	
Cores	9		6		20		14		14		14	

TABLE 4.4 FLIP-FLOP CORE AND WIRING TABULATION (Continued)

	Control Flip-Flops						Output Drivers					
	E		M		N		Sr		L_1		L_2	
	T	F	T	F	T	F	T	F	T	F	T	F
A												
B												
C									x			
I												
P									x			
R												
T												
F_1	x		x						x	x		
F_2												x
F_3	x	x	x	x	x	x						
F_4	x	x	x	x	x	x				x		
F_5	x		x	x	x				x	x	x	x
G	x		x	x					x		x	
J	x			x					x	x		
K_1	x	x	x						x	x		
K_2									x		x	x
K_3									x			
K_4									x	x	x	x
K_5										x		
K_6									x	x	x	x
E	x	x	x	x	x	x	x		x	x	x	x
M	x	x	x	x	x	x		x	x		x	x
N	x	x		x	x	x	x	x				
Sr		x			x		x				x	
Indep.												
$P_{inh.}$	1		1		1		1					
P_W	1		1		2				3		1	
P_R	1		1		2				3		1	
Mm	x	x	x	x	x	x						
C_W	x		x		x		x		x			
C_R	x		x		x		x		x			
Wires	24		23		21		8		30		17	
Cores	12		9		8		2		8		7	

TABLE 4.5 TABULATION OF NUMBER OF CORES LOGIC/MATRIX THREADED BY EACH P TIME CLOCK

	A	B	C	I	P	R	T	F_1	F_2	F_3	F_4	F_5	G	J	K_1	K_2	K_3	K_4	K_5	K_6	E	M	N	S_r	L_1	L_2
P_1	9							12	2	5	8	3	1	1												
$\overline{P}_1$	22	3						10	13	13	11	5		1												
P_2		1			1		2	2			2															
$\overline{P}_2$							2	2			3															
P_3									2																	
$\overline{P}_3$									2																	
P_4										2																
$\overline{P}_4$										2																
P_6							2				2															
$\overline{P}_6$							2																			
P_{14}								1							1										2	
$\overline{P}_{14}$								1							1											
P_{15}																1									1	
$\overline{P}_{15}$																1										
P_{16}																	2									
$\overline{P}_{16}$																	1									
P_{17}																		1								
$\overline{P}_{17}$																		1								
P_{18}																			1							
$\overline{P}_{18}$																			1							
P_{19}						1				1	22		1							1			1		3	
$\overline{P}_{19}$											4		2							1			1	1		
P_{20}		1						7	4	4	1	10			4	2	12	9	9	9	11	8	4			7
$\overline{P}_{20}$		4						9	13	8	7	10			2	1	4	3	3	3	1	1				

TABLE 4.5 TABULATION OF NUMBER OF CORES/LOGIC/MATRIX THREADED BY EACH P TIME CLOCK (Continued)

P logic pulses P_5, P_7 P_{13} have no load through them.

Total core load P time clock pulses.

	P_1	P_2	P_3	P_4	P_6	P_{14}	P_{15}	P_{16}	P_{17}	P_{18}	P_{19}	P_{20}	Total
Read -	41	8	2	2	4	4	2	2	1	1	30	102	199
Inhibit -	78	7	2	2	2	2	1	1	1	1	9	69	
Write and Inhibit -	119	15	4	4	6	6	3	3	2	2	39	171	374

layout can be finalized at the same time since the sense line threading is independent of the function order of the cores through which it passes. Table 4.6 shows the final tabulation of an acceptable matrix layout. Figures 4.16, 4.17, 4.18, and 4.19 present the particular matrix layout described in Table 4.6 with the final sense line configurations.

An examination of Table 4.6, which presents a matrix assignment and wire-per-module count for a single read clock system based upon the JPL logic lists, reveals that there are 24 wires which are common to all the modules. By running extra wires through those modules which have low required wire counts, the number of common wires may be raised to 33 without exceeding the specified goal of 51 wires per module. The extra wires are distinguished from the required wires, identified by the letter "X", by the use of the symbol "0". Thus the 30 pad sides of the module may be designated without regard to module function. This leaves only 34 wires and 14 pads to be assigned in accordance with the carrier board requirements.

4.6.4 Optimization Criteria for Individual Function Assignment

The only area left open to optimization at this phase of the design is that of minimization of active line driving voltage requirements. Since this voltage represents the load seen by the flip-flop and current driver outputs, it will determine both system power and driver fanout. The components of this voltage have been established in Paragraph 3.2. An examination of the voltage indicates that the unspecified variable is the length of each active line. Line length is entirely dependent upon the assignment of the logic tasks to the individual core and the assignment of the active terms to the input and output pads.

The means in which the minimum wire length criteria should be applied to the system depends upon the mechanization of the flip-flop outputs. If a floating switch is used so that several flip-flop outputs may be placed in series with a single current driver, minimization should be applied to the sum of all the inhibit lines in the worst-case configuration. Using this criteria complicates the problem considerably. On the other hand, if the flip-flop outputs are

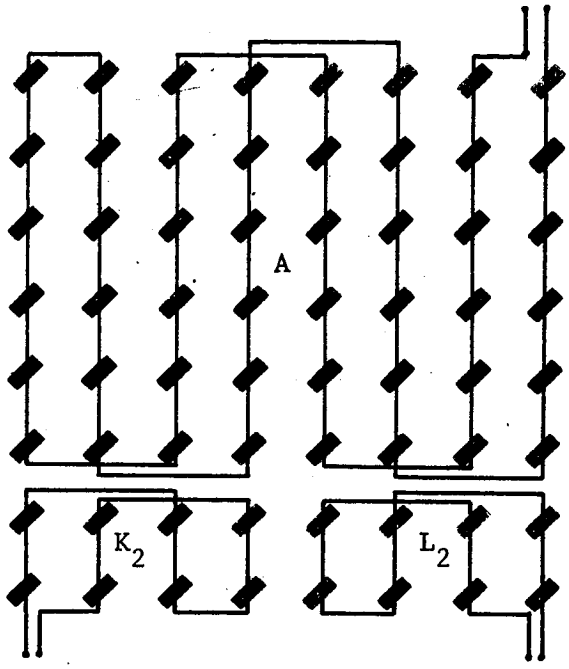
TABLE 4.6 FINAL MODULE LAYOUT CORE AND WIRING TABULATION
FOR A SINGLE READ CLOCK SYSTEM

Logic Matrices Per Module	A K_2 L_2		B K_4 K_5 K_6		P T I K_1		C R K_3 Sr		F_4		F_2 F_3 J		F_1 E G		F_5 L_1 M N	
Module No.	1		2		3		4		5		6		7		8	
Output Flip-Flop	T	F	T	F	T	F	T	F	T	F	T	F	T	F	T	F
A	x	x	x	o	o	o	x	x	x	x	x	x	x	x	x	x
B	x	x	x	x			x	x	x		x	x				
C	o		o		x	x	x		x	x	x		x		x	
I			x		x	x	x	x		x			x			
P					x	x			x		x				x	
R			x				x	x	x		x	x				
T	o	x	o	o	x	x	x	x	x	x	x	x	x	x	x	o
F_1	x	x	o		o		x	x	x	x	x	x	x		x	x
F_2	x	x	x							x	x	x				
F_3	x	x	x	x	x	x	x	x	o	o	x	x	x	x	x	x
F_4	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
F_5	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
G	x										x		x	x	x	x
J	x		o		x	x	o		x		x		x	x	x	x
K_1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
K_2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
K_3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
K_4	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
K_5	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
K_6	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
E	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
M	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
N		x		x	x	x	x	x					x	x	x	x
Sr	x				x		x	x					x	x	x	
Indep.	1												1		1	
P_W & $P_{inh.}$	3		5	1	4		4		5		5		5		5	
Sense lines	3		4		4		4		4		4		4		4	
Mm	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
C_W	x		x		x		x		x		x		x		x	
C_R	x		x		x		x		x		x		x		x	
No. of Cores Req.	61		55		59		63		60		63		63		54	
Wires Req.	46		43		47		50		47		51		51		50	
Wires used	48		49		50		51		49		51		51		51	

98

Module #1

Logic Matrices - A, K_2, L_2



Module #2

Logic Matrices - K_4, K_5, K_6, B

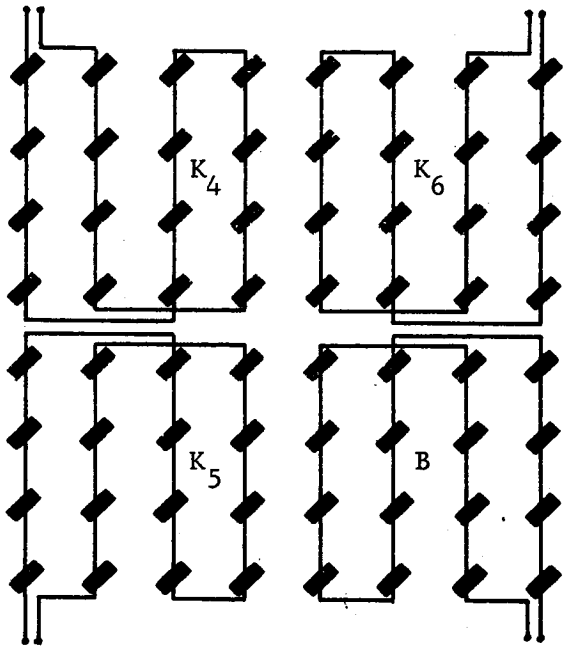
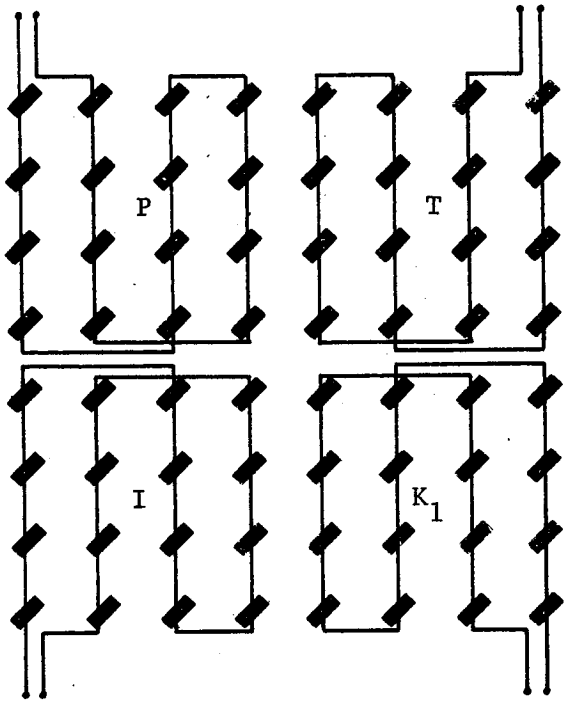


FIGURE 4.16 LOGIC MATRIX AND SENSE LINE LAYOUTS FOR MODULE #1 AND MODULE #2

Module #3

Logic Matrices - P, T, I, K_1



Module #4

Logic Matrices - R, C, S_r, K_3

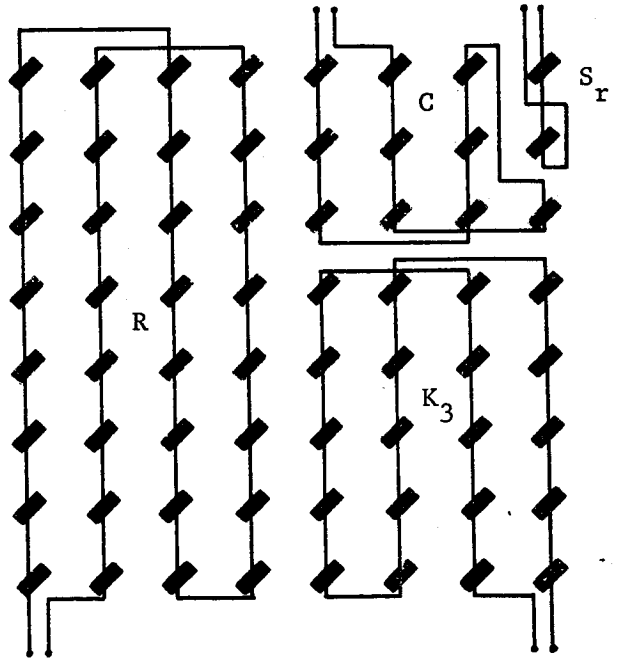
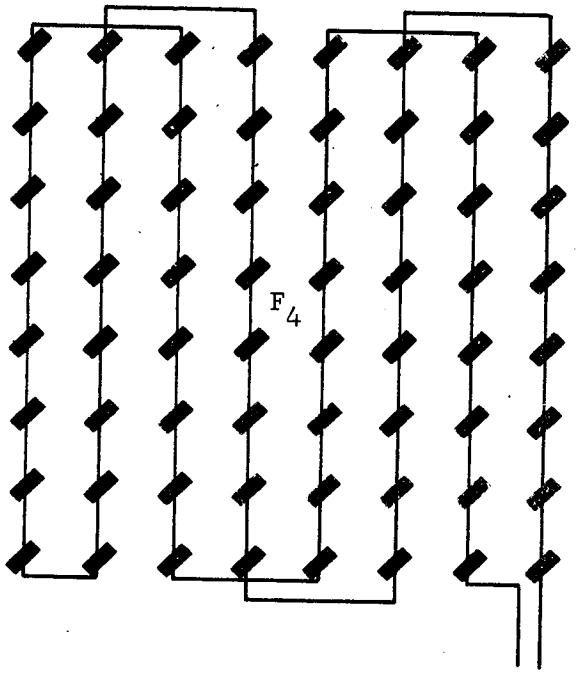


FIGURE 4.17 LOGIC MATRIX AND SENSE LINE LAYOUTS FOR MODULE #3 AND MODULE #4

Module #5
Logic Matrices - F_4



Module #6
Logic Matrices - F_2, F_3, J

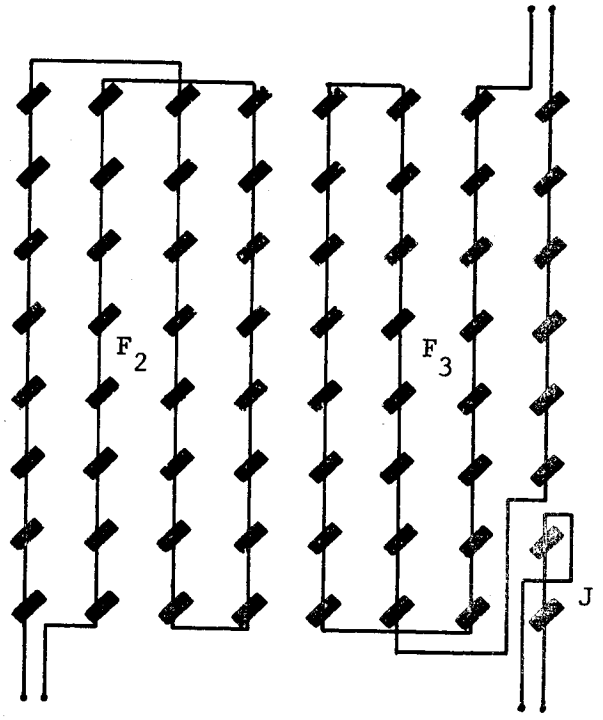
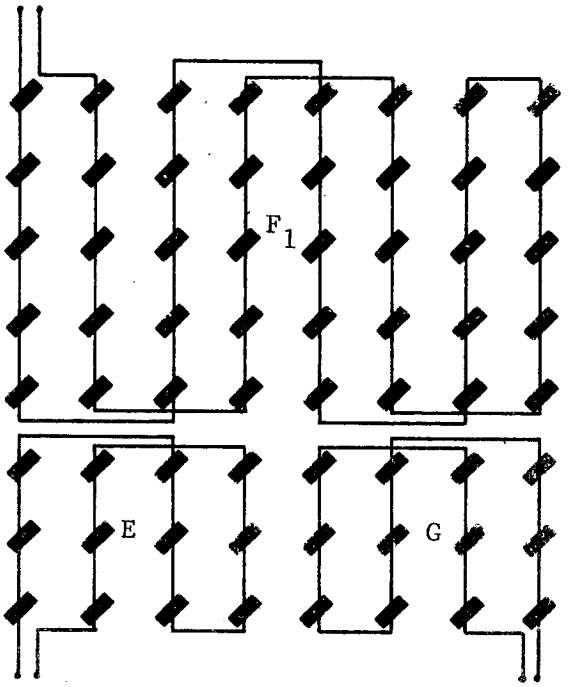


FIGURE 4.18 LOGIC MATRIX AND SENSE LINE LAYOUTS FOR MODULE #5 AND MODULE #6

Module #7

Logic Matrices - F_1, E, G



Module #8

Logic Matrices - F_5, M, L_1, N

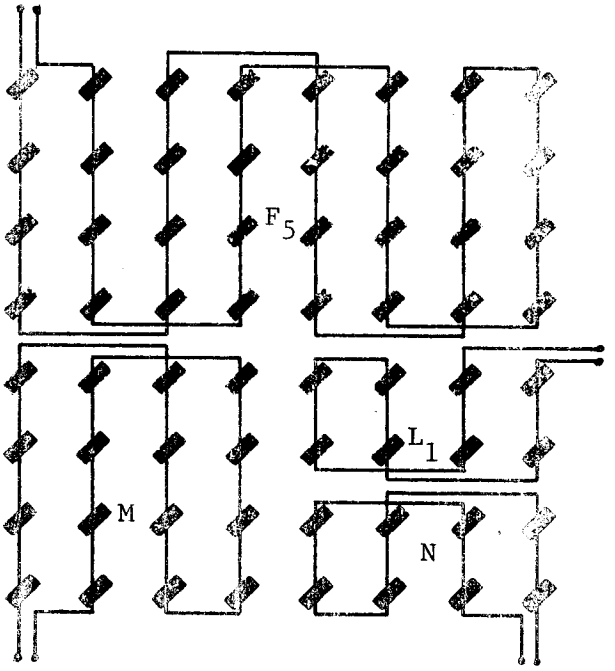


FIGURE 4.19 LOGIC MATRIX AND SENSE LINE LAYOUTS FOR MODULE #7 AND MODULE #8

mechanized as fixed reference switches, it is necessary to minimize the length of the most heavily loaded wire to achieve an optimum configuration. The advantages of one system over the other probably lie in the efficiency of the switches required to mechanize them, since the matrix power for the two systems will probably not vary significantly. The present JPL magnetic switch probably represents the worst efficiency available since it represents a greater flux load than the worst-case line it has to drive.

A method for mechanizing the minimization of the longest single line can be demonstrated. The problem will not be pursued further in this report, however, because the inadequacy of the present system may require changes which would invalidate the complete procedure. The degree of optimization that can be achieved by a special ordering of the cores has not been demonstrated. It may become evident that the effort required by such a process could not be justified by material gains.

4.6.5 Computer Mechanization of the Wire Routing Problem

To insure the accuracy of the production wiring lists, it is recommended that the lists be programmed on a general purpose digital computer. A computer mechanization of the wire routing problem may serve as a basic bookkeeping aid, which is easily changed and verified, and to generate wiring aids and production verification tapes free of transcription errors. The possibility of including in this program a wire length optimizing routine can substantially increase the program value by converting it into a powerful design tool.

The general wiring optimization problem has been the subject of study by Bellman, Dantzig, Lee, and others who set out to solve the "shortest-route traveling salesman" problem and apply its solution to a general point-to-point wiring situation. The traveling salesman problem is stated as follows: "A salesman is required to visit once and only once each of n different cities starting at a base city and ending at a terminal city. What path may the salesman take to minimize his total distance traveled?" In the present situation the cities to be visited between the base and terminal cities represent the cores and the base and

terminal cities represent the input and output pads respectively. It will be assumed that the positions of these points are known although certain general positioning steps which take into account the overall wiring problem will be introduced later.

The function $f(S, j_1, j_2, \ldots\ldots j_k, E)$ is defined as the length of a path which starts at pad S, passes once and only once through each of K cores (j), and ends at pad E. To tabulate this function it is necessary to account for the totality of wired cores j_1 through j_k. However, to find a minimum length, it is necessary to examine all possible tabulations and compare them. The number of combinations which are available increases as the factorial of K and therefore approaches astronomical numbers as the number of cores increases. Any set of restrictive wiring rules such as those proposed for the present system can be employed to reduce the number of solutions available. The number of decisions required drops rapidly as the rules become more restrictive.

If no limiting rules are incorporated, the number of computations must be kept within the bounds dictated by economy and computing system capability by other methods. One alternative is to section the matrix into smaller groups of cores which may be treated individually. The criteria employed in this partitioning operation may, if properly chosen, lead toward a partially optimum solution. Among the criteria open for use, three are listed.

1) Grouping according to the maximum number of logic terms per core.
2) Grouping according to the minimum number of logic terms per core.
3) Grouping according to the similarity of the logic terms threading the cores.

It may be desirable to use several different criteria at different levels in the process. The module matrices may first be sectioned according to the maximum number of wires per core, and then positioned within the groups according to the similarity of the terms threading these cores with other cores of the same group or with cores of other groups. The process may be refined as much as desired; however, it appears almost impossible to determine at what level the process costs begin to outweigh the optimization gains. Figures 4.20 and 4.21 present a flow chart which describes this process.

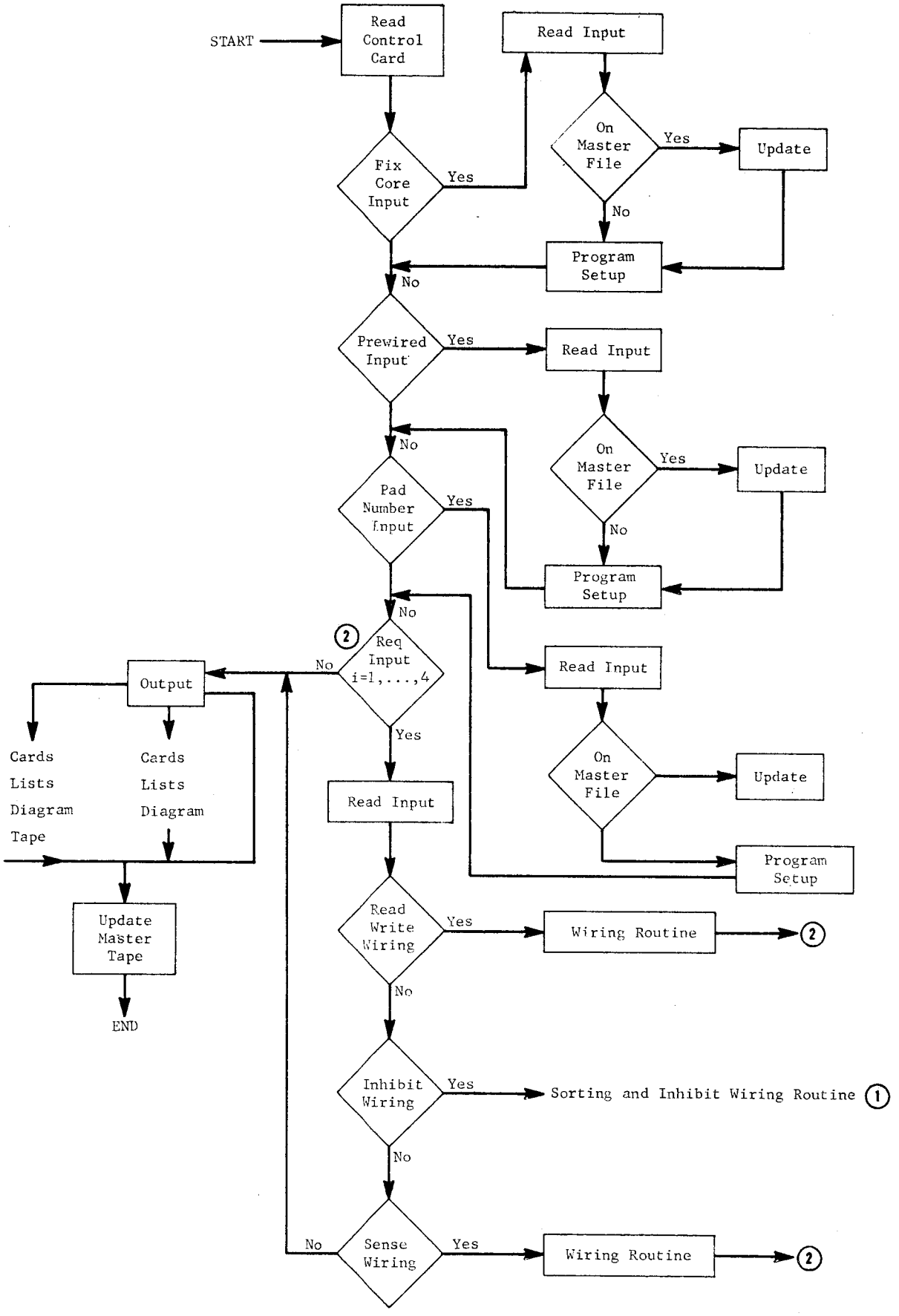


FIGURE 4.20 PROGRAMMED PROCEDURE

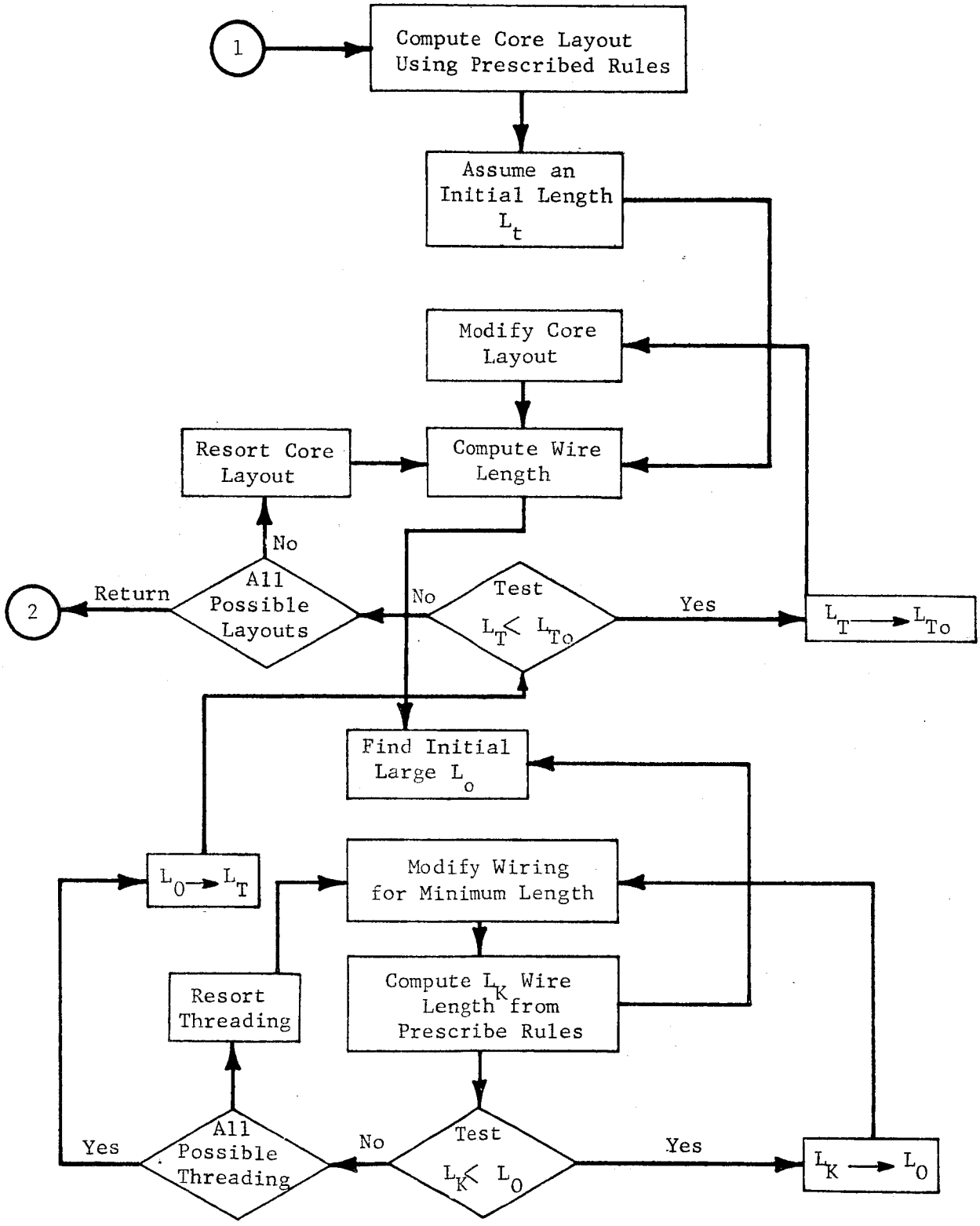


FIGURE 4.21 SORTING AND INHIBIT WIRING ROUTINE

The present packaging situation prescribes a very restrictive set of wiring rules. Under these rules both core arrangement and wire routing become a relatively straightforward computation task. By laying the cores out in a sequence determined by maximum number of cores threaded by a single logic term, an optimization can be reached which insures at least that the most heavily loaded logic terms (those threading the most cores) are threaded with a minimum of wire. The actual threading process has been considerably simplified by the fact that the cores are treated in groups of four each. This reduces the number of decisions required from a possible 64 to a maximum of 24. The number of alternatives available at each decision point has been reduced to a maximum of 16 and the rules for making a decision may be established. These facts are plainly evident from an examination of the wiring rules presented in previous sections and will not be discussed further.

The input format recommended for mechanizing the wire routing problem on an IBM 7090 computing system is illustrated in Figure 4.22. It was derived from an examination of the logic list presented in JPL Memo No. 341-32 by David Rubin. Two types of input cards are required of which the first is obviously a data input card. The second, called the control card, is provided to help simplify the handling of large amounts of data required by this type of problem by giving input and execution control of this program to the programmer.

The basic output format recommended for the program printout is shown in Table 4.7. This will provide a complete wiring record and, if necessary, can be used to generate the wiring aids and production tester tapes directly. The printed wire list for each term will include the following information:

1) Logic term sequence number
2) Logic term name or abbreviation
3) Input pad number
4) Output pad number
5) Cores and core position coordinates.

The columns are labeled from left to right as A, B, C ... H; the rows are numbered from 1 to 8, starting at the top.

KEY PUNCH FORM - GENERAL PURPOSE

FORM 20-708 (R.1-60)

JOB TITLE				ENGINEER	PAGE 1 OF 2
A/C CODE / DIV. / SALES ORDER / DASH	EWO NO.	FOR ORGN. NO.		ANALYST	DATE

Fix Core Input
Prewired Input
Pad Number
Number of Cores
Register Name
Type Wiring
Output Indicator
Date
Deck Number

0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 5 5 5 5 5 5 5 5 5 6 6 6 6 6 6 6 6 6 7 7 7 7 7 7 7 7 8
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0

1 2 3 4 a 5 b 6 c 7 d 8 01 / 16 / 63

I. Control Card

1. Fix Core Position Input - 2 = Yes, Blank = No
2. Prewired Input - 1 = Yes, Blank = No
3. Pad Numbers Input - 1 = Yes, Blank = No
4, 5, 6, 7 Number of Cores in each Register - 1, 2, - - - , N
a, b, c, b Register Name - A, B, F1, F2, - - -
8. Type wiring - Read, Write, or Sense
9. Output Indicator - 1 = Punch Cards, Wire List, Diagram, Tape Format
Blank = Punch Cards, Wire List, Diagram
0 = No Output
10. Date

Data Input

I a b a No. of cards for fix core position input, b Register

1 2 3
1 Core Number — Data for fix core position
2 X = Column of Matrix
3 Y = Row of Matrix

II b c b No. of cards for prewired cores, c - - - - - - - - Prewired Register No

1 2 3
1 Core Number — Data for Prewire Cores
2 X = Column of Matrix
3 Y = Row of Matrix

4-50

NORT 63-45

8/1/63

KEY PUNCH FORM - GENERAL PURPOSE

FORM 20-708 (R.1-60)

JOB TITLE				ENGINEER	PAGE 2 OF 2
A/C CODE / DIV. / SALES ORDER / DASH	FWO NO.	FOR ORGN. NO.		ANALYST	DATE

Fix Core Input
Prewired Input
Pad Number
Number of Cores
Register Name
Type Wiring
Output Indicator
Date
Deck Number

```
0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 5 5 5 5 5 5 5 5 5 6 6 6 6 6 6 6 6 6 7 7 7 7 7 7 7 7 7 8
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0
```

1 2 3 4a 5 b 6 c 7 d 8 01 / 16 / 63

II c = Number of cards for pad number or name

1 2 Data for pad numbers

1 2 - - - - Number or name of pads

IV d Logic Register Inputs

1 2 3 Data for register inputs

1 Core Number

2 Continuation of logic terms of previous core - 1 = Yes, Blank = No

3, 4 - - - - Logic terms for the core

$ = End of terms for core

9999 = End of cores for register

4-51

NORT 63-45

109

TABLE 4.7 WIRING PROGRAM OUTPUT FORMAT

1. Logic Term Number = ( )
2. Logic Term Name = ( )
3. Beginning Pad Number = ( )
4. End Pad Number = ( )

Begin Term	From *x y	± Core No.	*x y	± Core No.		End x y	± Core No.	Type Wire	Length

Begin term - Pad Number

* From - x, y coordinates of start point

Core No. - Core number (1, 2, -)

* Via - x, y coordinates of core to be threaded

Note: "+" core number core is wired from left to right, "-" core number core is wired from right to left

Type Wire - Wire type -

Length - Total Length of wire.

This sheet is printed for each term to be wired.

* x = 1, 2, 3, --- 8

y = A, B, C, --- H

An investigation should be made into additional routines which might be added so that the overall program may be developed into a powerful production tool. The first such routine would generate the production test equipment tapes. This tester insures that the logic wires which string the matrix conform to the logical equations specified by the logical designer. It is an absolute necessity that these tapes be correct. A computer routine for generating and verifying the tapes could prove to be the most worthwhile task of the wiring program.

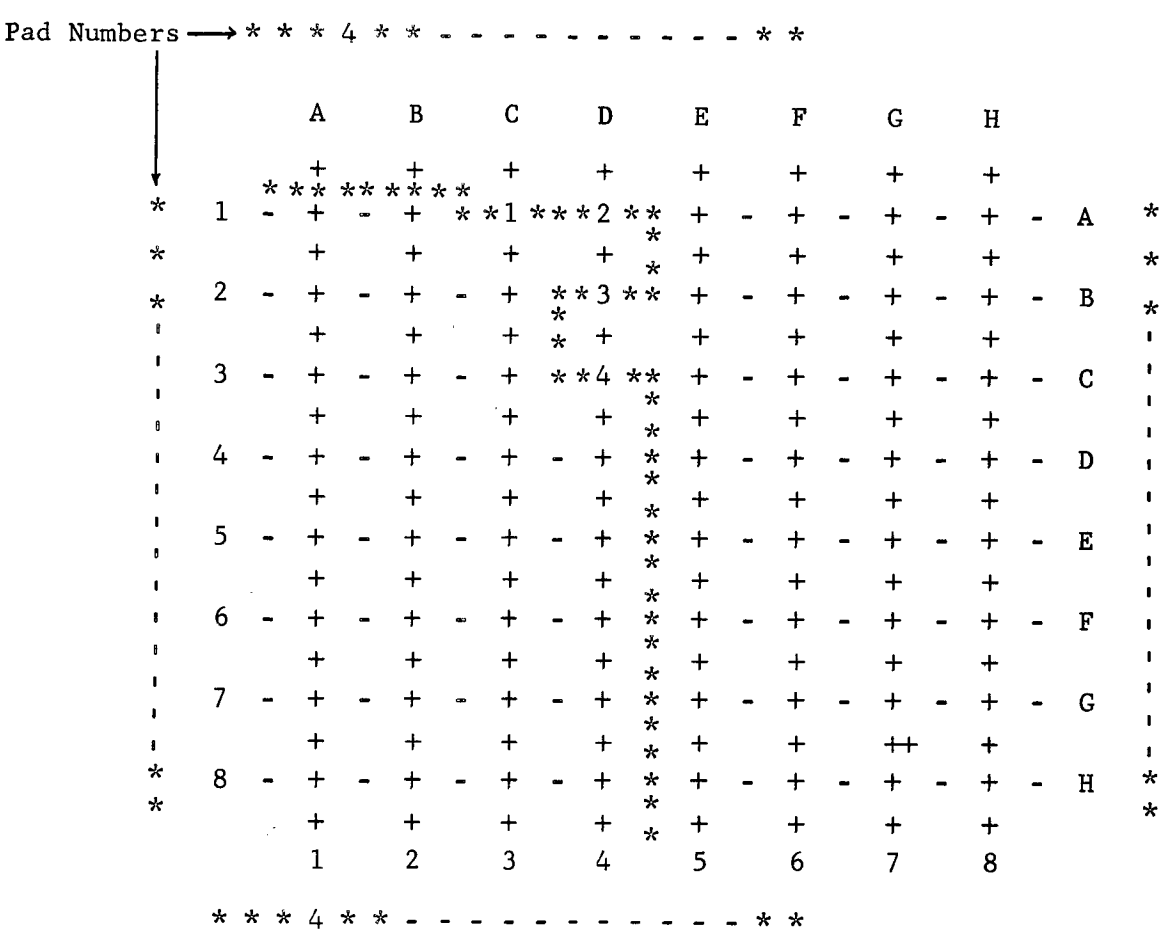
Another area in which the wiring routine may be expanded to cover a useful function is that of production wiring aid development. The computer can be programmed to provide a picture of each wire as it threads the matrix. The format that these graphs might take is illustrated in Figure 4.23.

There are many other uses for a wiring program. The printing of information pertinent to each module on the face of each wiring diagram, and the computation of overall wire lengths for use in the wire cutting and stripping process could be effectively mechanized. Unfortunately, this study program was limited to a broad coverage of computer wiring routines and could not afford time for detailed studies of each.

4.7 Packaging Study Conclusions and Recommendations

4.7.1 Conclusions

It became quite evident in the early stages of this study that the characteristics of the JPL ferrite core used as the basic logic element in the system would present the most serious barriers to the achievement of an optimum packaging configuration. The discussions in Paragraphs 4.3, 4.4, and 4.5 show quite clearly that this has been the case. In almost every decision the core's surface characteristics or size became the major determining factor. It is felt that the enormity of the sacrifices made to accommodate this particular element far outweighs any advantages it may have. The availability of metallic tape-wound bobbin cores which are much easier to handle from the packaging standpoint would permit an element substitution which would considerably simplify the proposed system and could lead to a substantially improved system.



The notation used in Figure 4.23 is defined below.

1. The pads which are not connected with this term are indicated by "*" asterisk. The pad number or name will be printed in the location where the term is connected.
2. Columns (A, B, C, - - - - H) of the matrix are drawn with "+".
3. Rows (1, 2, - - - - - 8) of the matrix are drawn with "-".
4. Intersection of the rows and column are core position.
5. The wire to be threaded is indicated by a sequence of * (asterisk) between the rows and column to the intersection of the core position it is to thread.
6. The direction of the wire through the core is also indicated by the asterisks (see example).
7. At this intersection the number of the cores to be wired is printed in ascending order (i.e.), 1, 2, 3, ... , n.

FIGURE 4.23 ILLUSTRATION OF COMPUTER GENERATED WIRING AID

In spite of the discussion presented above, the recommended package as presented in Paragraphs 4.3, 4.4, and 4.5 adequately satisfies the present requirements. A brief summary of these recommendations is presented below.

1) That the basic module contain an 8 x 8 square core array with the cores oriented in an upright position and a uniformly diagonal direction relative to the x and y axes of the basic circuit board. (See Figures 4.1 and 4.2.)

2) That the basic circuit incorporate stress relief pins as shown in Figure 4.5.

3) That #38 AWG heavy formvar insulated copper magnet wire be used for core wiring.

4) That #30 AWG heavy formvar insulated copper magnet wire be used for the x/y test selection wires.

5) That standard high-reliability hand-soldering be employed for all electrical connections.

6) That high melting point solder (Sn 50) be used for internal module wire to pad connections and eutectic (Sn 63) low-temperature solder be used for connecting the modules into the memory subsystem.

7) That individual memory modules be protected in a combination silastic-epoxy system of RTV 11 and Scotchcast 241. (See Figure 4.2.)

8) That the modules be married to a two-sided interconnection board as shown in Figures 4.6 and 4.7.

9) That the cores be coated prior to assembly to reduce abrasive characteristics of core material.

10) That chemical stripping using Lonco 3111 stripping agent followed by ultrasonic cleaning and neutralization be used for removal of insulation from magnet wire.

11) The procedure for generating the final module wiring lists should be mechanized on a digital computer. The advantages in such a system once established would far outweigh the time required to program such a problem. Even if optimization criteria are not built into the program the power of such a tool as a bookkeeping procedure makes it a worthwhile endeavor. The possibility of incorporating into such a program such features as production aid graphing, production tester tape verification, and production tester tape generation makes it seem to be a near necessity.

4.7.2 Recommendations

The poor volume efficiency faced in the present system could be significantly improved by allowing a change in the basic form factor required by the subassembly configuration. The matrix may be folded into a stacked configuration as shown in Figure 4.24 without any significant change required of the module. The dimensions of this memory organization are approximately 3.5 inches by 2.6 inches by 3.0 inches versus the subassembly dimensions of 1 inch by 6 inches by 14 inches. The volume ratio of this improved configuration to the original is approximately 1 : 3 . An improvement of this magnitude should make the system seem considerably more attractive. The wiring of the 30 pad sides of the modules could be accomplished point-to-point without any change in pad assignment since the wires are common to every module. The wiring of the 20 pad sides of the modules can be made easier by a proper assignment of pad tasks and a proper ordering of the modules. It can be seen here that the present system can be improved considerably in terms of volume efficiency.

The most beneficial change which could be made in the present system would be to substitute a metallic tape-wound bobbin core for the basic logic element. The mechanical characteristics of this core are more suitable to the mechanization of inhibit core logic. The surfaces are non-abrasive, the corners are smooth, and the magnetic material is fully protected by a bobbin and sleeve combination. The bobbin material is conductive but the cores may be bought pre-coated with an insulating material. The core threading window is considerably larger for core sizes which might be considered. Even though this core is larger, its

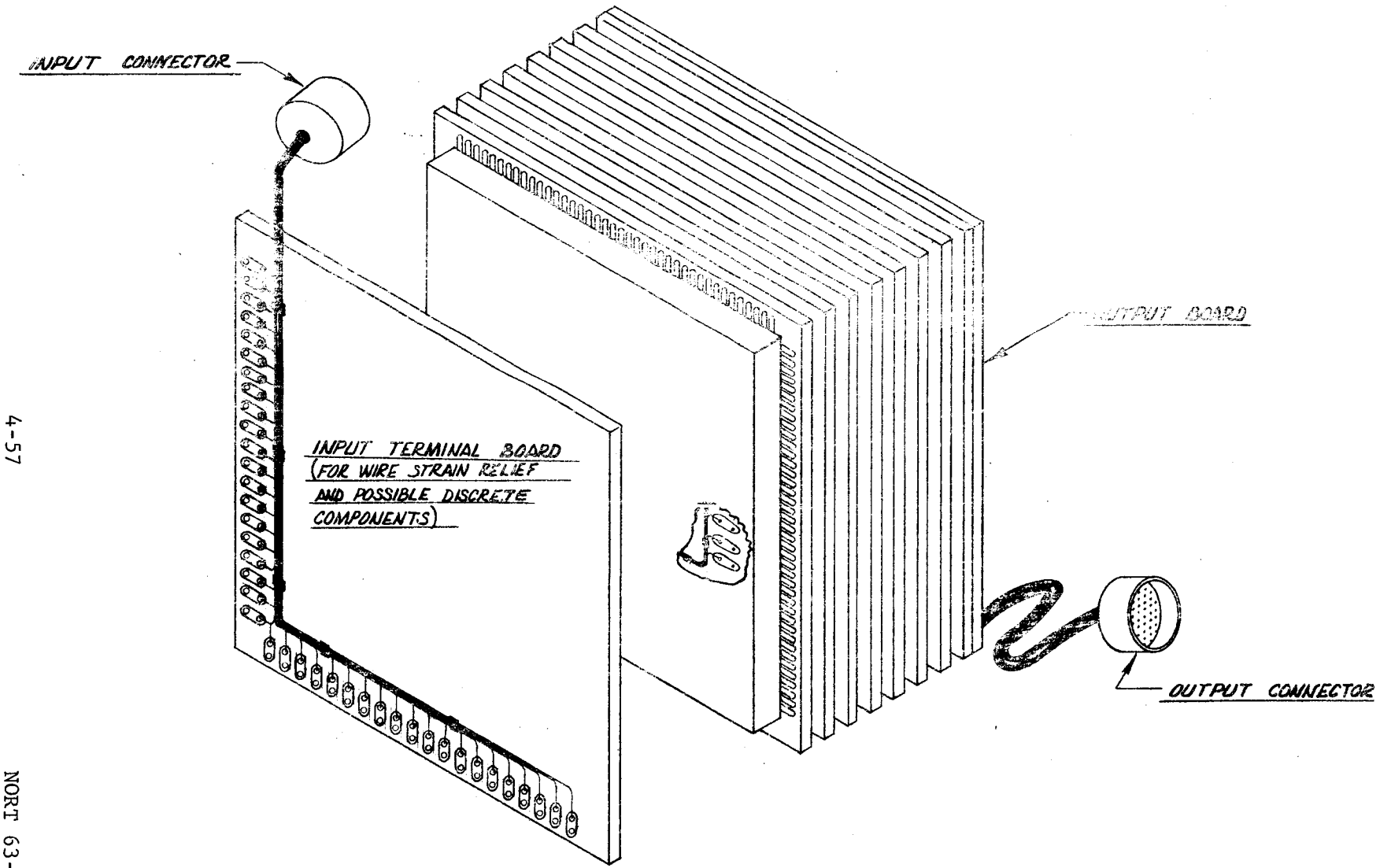


FIGURE 4.24 RECOMMENDED MINIMUM VOLUME MEMORY CONFIGURATION SHOWING 8 MODULE STACK, 64 CORES PER MODULE

advantageous mechanical characteristics would allow at least a doubling of the number of cores per module. This permits another significant volume reduction of the overall memory size. It may be possible to go to a single matrix of 500 cores which represents the limit in volume efficiency and minimization of wire lengths. An increase in wire size to No. 36 or No. 34 should be possible without exerting additional strain on the wiring process. For these reasons and others not mentioned, the switch from ferrite to metallic tape for the logic element core material would seem to be most judicious.

5. PRODUCTION AND MAINTENANCE TEST EQUIPMENT

5.1 Production Test Equipment

The purpose of the production test equipment is to provide production personnel with an efficient and reliable means of determining the correctness of the wires threading a logic matrix card. The equipment shall have the capability to perform the tests at any stage in the production process without disrupting the operator.

5.1.1 Testing Methods

Because the complexity of the wiring of a logic matrix (approximately 50 wires randomly threading 60 cores) it is desirable that the production test equipment be capable of performing a wiring test at any stage in the production process. This test should ensure that each term linking a matrix threads the proper cores in that matrix. The wiring tests could be performed after a group of terms are threaded or after each individual term is threaded. To reduce the problem of wire abrasion, it is recommended that a wiring test be performed upon each individual wire as it is threaded.

Some method of detecting a wiring error must be devised to eliminate the need for visually inspecting a wire route for correctness. It is assumed that production personnel will be working with cores which have passed an incoming inspection test to ensure proper switching characteristics. Each matrix may contain a maximum of 64 cores arranged in an 8 by 8 matrix. To support the cores during the threading process and to provide a means of electronically selecting individual cores, a standard "X" and "Y" wire grid will be utilized. After each term is threaded, the cores in the matrix are pulsed sequentially with a write/read current program utilizing the grid system for selection. A "one" output voltage will appear on the wire if the selected core is threaded by the wire. A "zero" voltage will appear if the term does not thread the selected core. Therefore, the inhibit term itself may be utilized as a sense line to determine that proper threading exists.

The matrix positions of the cores threaded by a term are contained in the wire lists. Electronic comparison of the threaded route and the desired route may be accomplished utilizing some form of auxiliary storage.

5.1.2 Test Equipment Implementation

5.1.2.1 Selection Technique: The logic cores will be assembled in a matrix as shown in Figure 5.1. The matrix will contain a maximum of 64 cores threaded with "X" and "Y" selection wires as shown. There are many possible methods of selecting one core from the total number. The most favorable from the standpoint of minimum hardware and induced noise is to bias seven of the eight "X" wires with sufficient current to ensure that the cores are heavily saturated (see Figure 5.2). The remaining eight cores are sequentially pulsed with a write/read current program. A selected core will be switched from one remanent state to the other and a "one" signal will appear on the wires threading the core. A "zero" signal will appear on the wires if the term does not thread the selected core. This "zero" signal will be the result of shuttle flux change induced from the saturated cores threaded by the term. The signal-to-noise ratio will be sufficiently large to permit detection of the "one" signal and discrimination of the "zero" signal.

To select one core from the 64, eight "X" bias drivers and eight bi-polar "Y" drivers are required. The eight bi-polar current drivers may be factored into a 2-driver/4-switch configuration (see Figure 5.3), thereby reducing the number of current drivers required. A six-bit register and driver decoder will be required to store the selected address and to activate seven bias drivers and one bi-polar current driver and switch. Decoding may be accomplished by diode gates inserted at the input of the drivers and switches. The six-bit address register must be capable of driving at least eight gates.

5.1.2.2 Bi-Polar Sense Amplifier: A sense amplifier will be required to detect the "one" or "zero" signals and the polarity of the "one" signal. The polarity detection feature is required due to the manner in which the inhibit terms thread the matrix and the use of P-time lines as inhibit and/or clock terms. The cores of the matrix will be tested devices, and therefore, the minimum output signal for a given ambient temperature will be known. The amplifier should be capable of indicating a "zero" signal for input signals lower than this minimum acceptable level. Strobing the output of the sense amplifier will ensure an acceptable core peaking time. A simplified block diagram of a typical amplifier is shown in Figure 5.4. The polarity detection feature is accomplished through rectification.

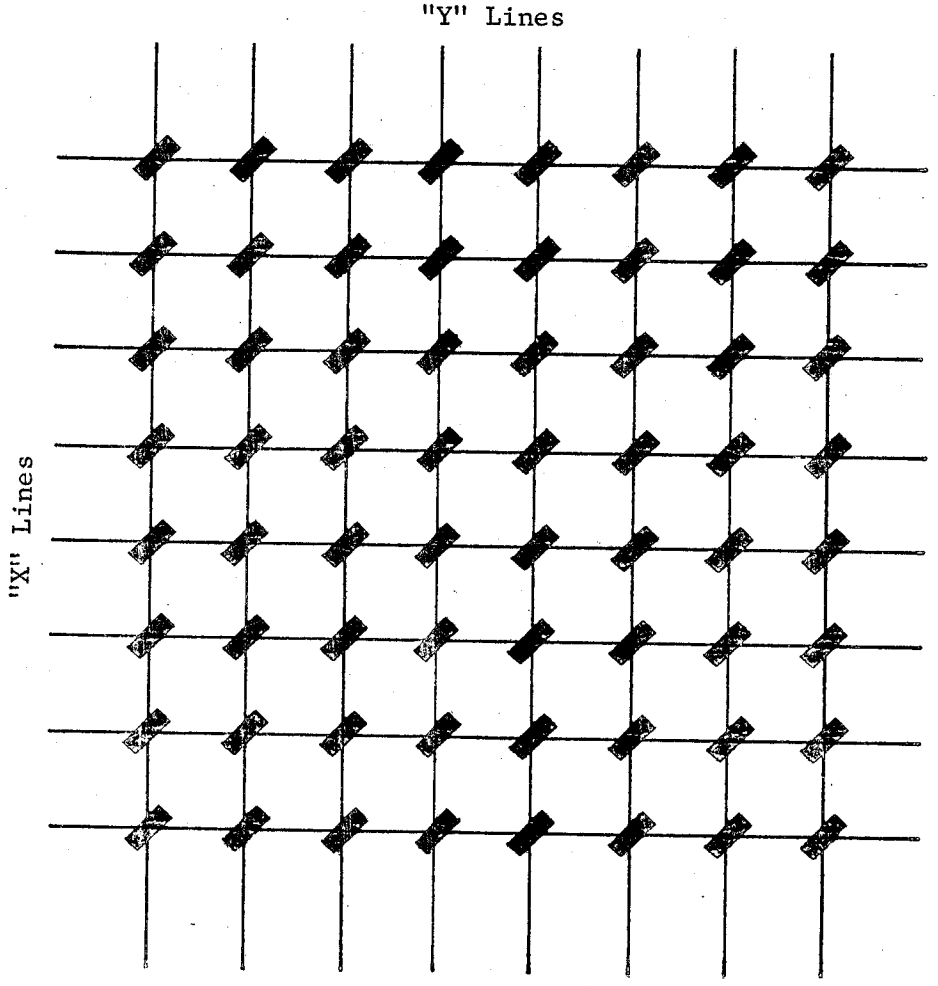


FIGURE 5.1 CORE MATRIX SELECTION LINE DIAGRAM

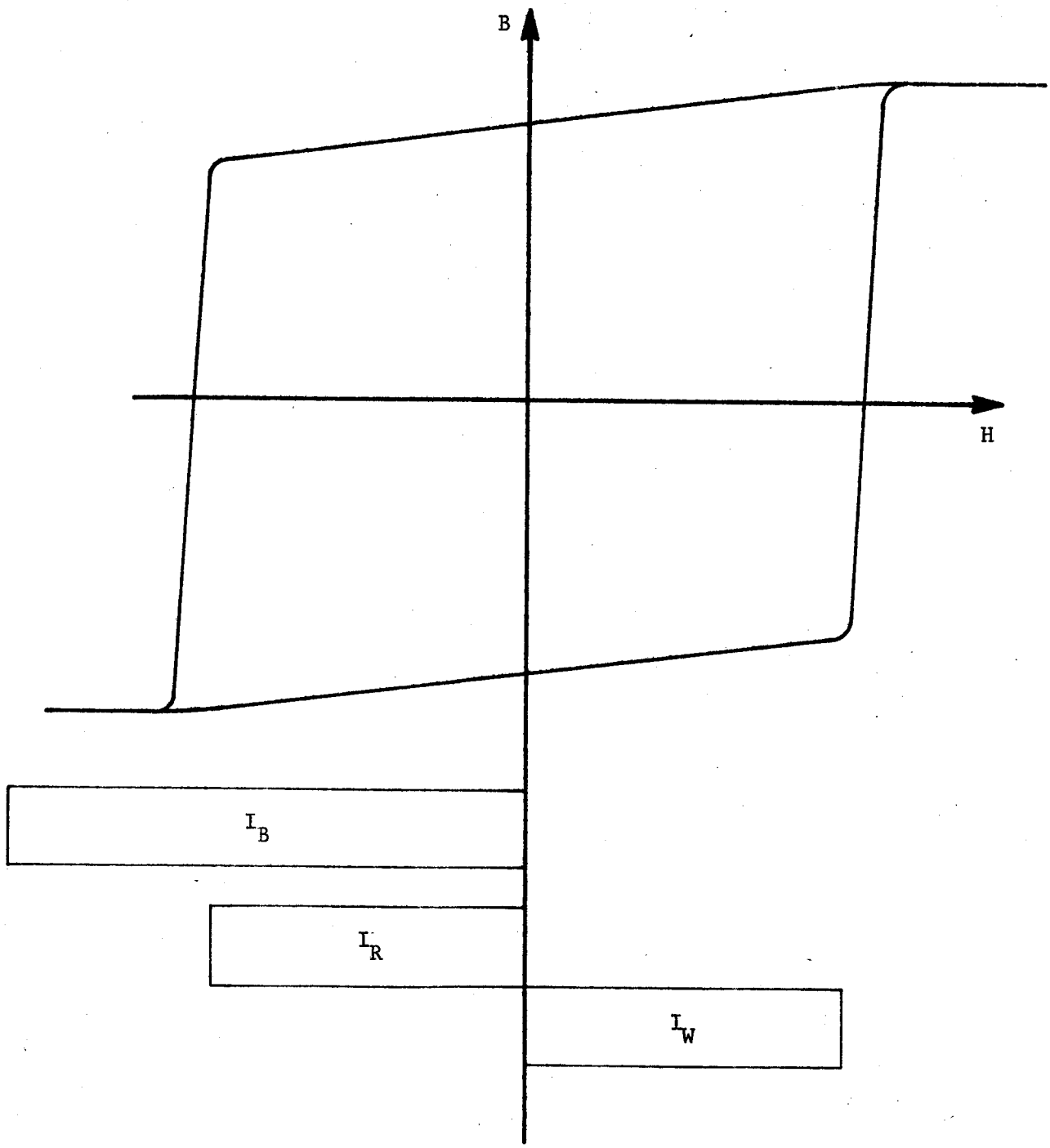


FIGURE 5.2 TYPICAL CORE HYSTERESIS LOOP SHOWING I_B, I_R AND I_W

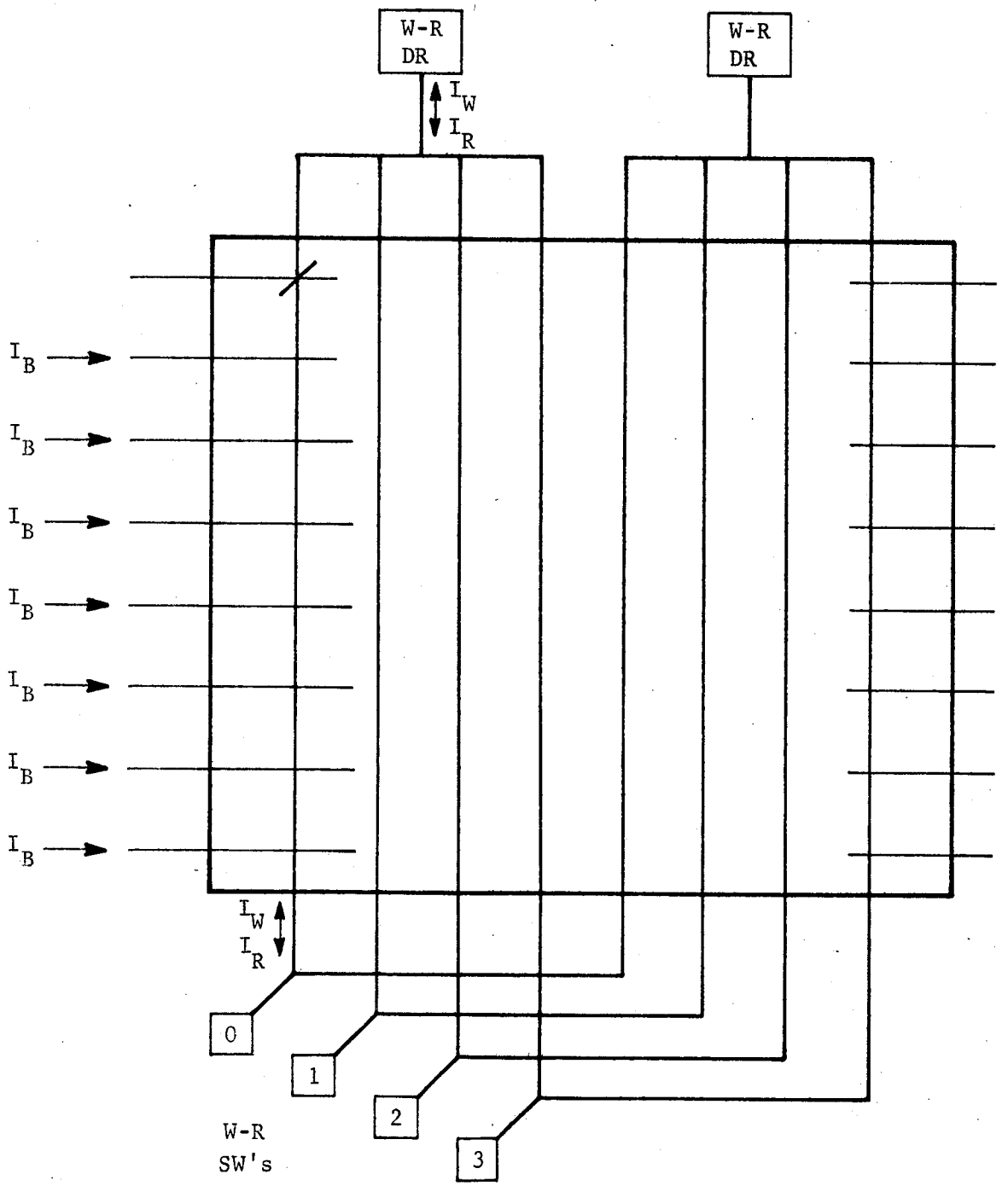


FIGURE 5.3 MATRIX SELECTION METHOD SHOWING SELECTION OF CORE 0-0

NORT 63-45

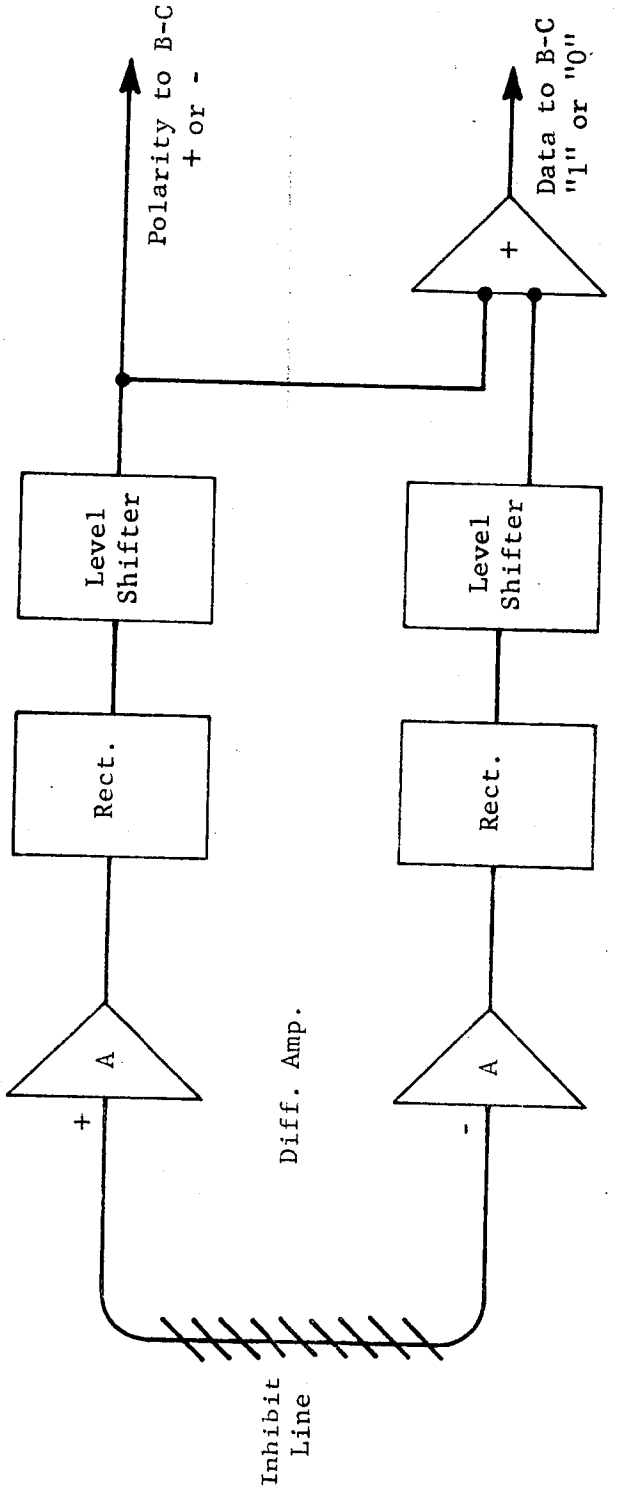


FIGURE 5.4 SENSE AMPLIFIER - BLOCK DIAGRAM

The sense amplifier will contain a differential amplifier section, a rectifier section for polarity detection, and an output amplifier to restore the rectified core signal to a logic level. The gain of the amplifier will be adjustable. The amplitude of the output strobe signal will be variable in amplitude for voltage level discrimination. Since the test operation is serial in nature, only one sense amplifier will be required. This circuit may be designed to as high a degree of sophistication as is necessary to ensure proper matrix operation.

5.1.2.3 Buffer-Comparitor: The Buffer-Comparitor will be required to store the data received from auxiliary storage and compare this data with that received from the sense amplifier. Two flip-flops are required for storing the bit data (one or zero) from the auxiliary storage and the sense amplifier and two flip-flops for storing the polarity information. Comparison may be accomplished by two exclusive OR circuits that drive an "and" gate. The "and" gate will be strobed and its output transmitted to an error flip-flop in the Timing and Control section.

5.1.2.4 Timing and Control: The Timing and Control section of the test equipment is required to generate all timing pulses necessary to cycle one core in the matrix and to control the auxiliary storage. The following timing pulses are required:

1) Bias driver timing

2) Write/read timing

3) Sense amplifier timing

4) Comparitor timing

5) Input data timing.

The timing pulses are representative of a typical system and addition or deletions will be dictated by the type of auxiliary storage utilized.

The control functions required are start test, stop test, stop test-comparitor error, and error override.

5.1.2.5 Auxiliary Storage: Any form of auxiliary storage with a capacity of approximately 26,000 bits (50 x 64 or 3200 words of 8 bits per word) would be compatible with the test system. However, since the speed of operation is of little

consequence, a paper tape reader is adequate and the least expensive. A tape would be prepared for each logic matrix card. A minimum of eight bits of data per core location would be required. The address is determined by six bits and the core data by two bits ("one" or "zero," plus or minus for polarity). It would be advantageous to have the tape reader capable of not reading the next character after receipt of an error signal. Mechanical readers will usually meet this requirement.

Should stopping the reader become a problem, the characters may be widely spaced. If the reader does not contain a sprocket hole for clocking of information, the following scheme will afford a clock pulse: - Two holes are required for core data (one hole to determine if the wire threads the core and one hole to determine whether the polarity is plus or minus). Define the threading of a core as a "one." Define plus polarity as a "one." If the core is not threaded, the data hole is a zero and polarity is meaningless. Therefore, the polarity hole is always punched if the data hole is zero and the two holes are connected to an OR gate. The output of this gate will then furnish a system clock. A typical timing program for the overall system is shown in Figure 5.5.

It would be advantageous if the equipment were capable of a manual mode of operation. If an error occurs, the reader would stop and the faulty address would remain in the address register. The operator would shift to manual and observe the sense amplifier input. This would require an address register manual toggling capability and a system clock for manual mode.

5.1.2.6 System Operation: (See Figure 5.6.) The matrix card may be wired in a test fixture interconnected to the test equipment or transferred to the fixture after each term has been threaded. The tape prepared for this card is placed in the reader and the checkout run is started. The data and address is transferred to the address register and buffer-comparitor during data input time. The bias drivers are enabled, and the write/read clocks are generated. The selected core is pulsed and the sense amplifier detects the output and transfers this information to the buffer-comparitor. The output of the buffer-comparitor is transferred to the error flip-flop at comparison time. If no error exists the next address is read. If an error exists the reader is stopped and the faulty address is indicated

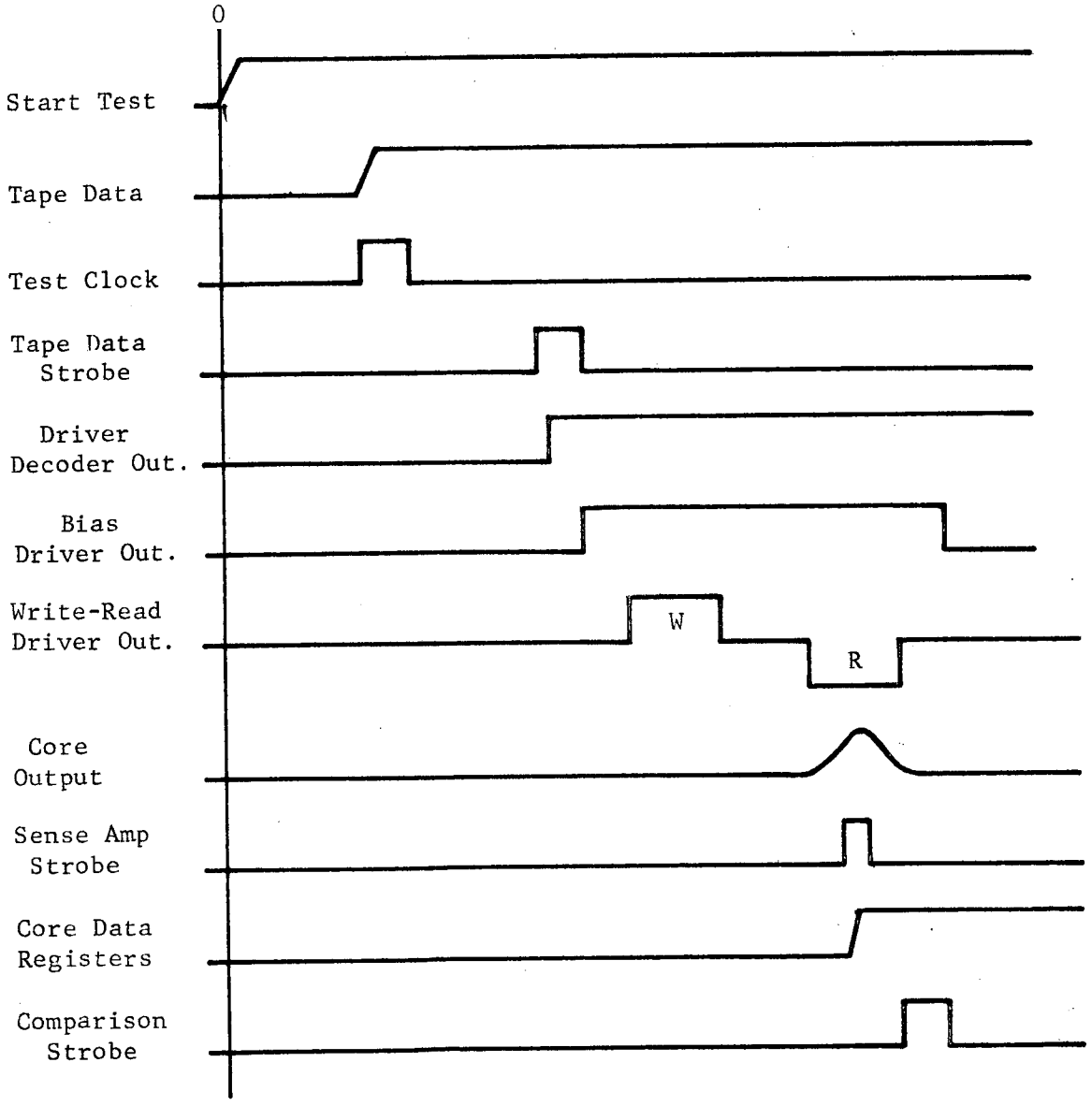


FIGURE 5.5 PRODUCTION TESTER TIMING DIAGRAM

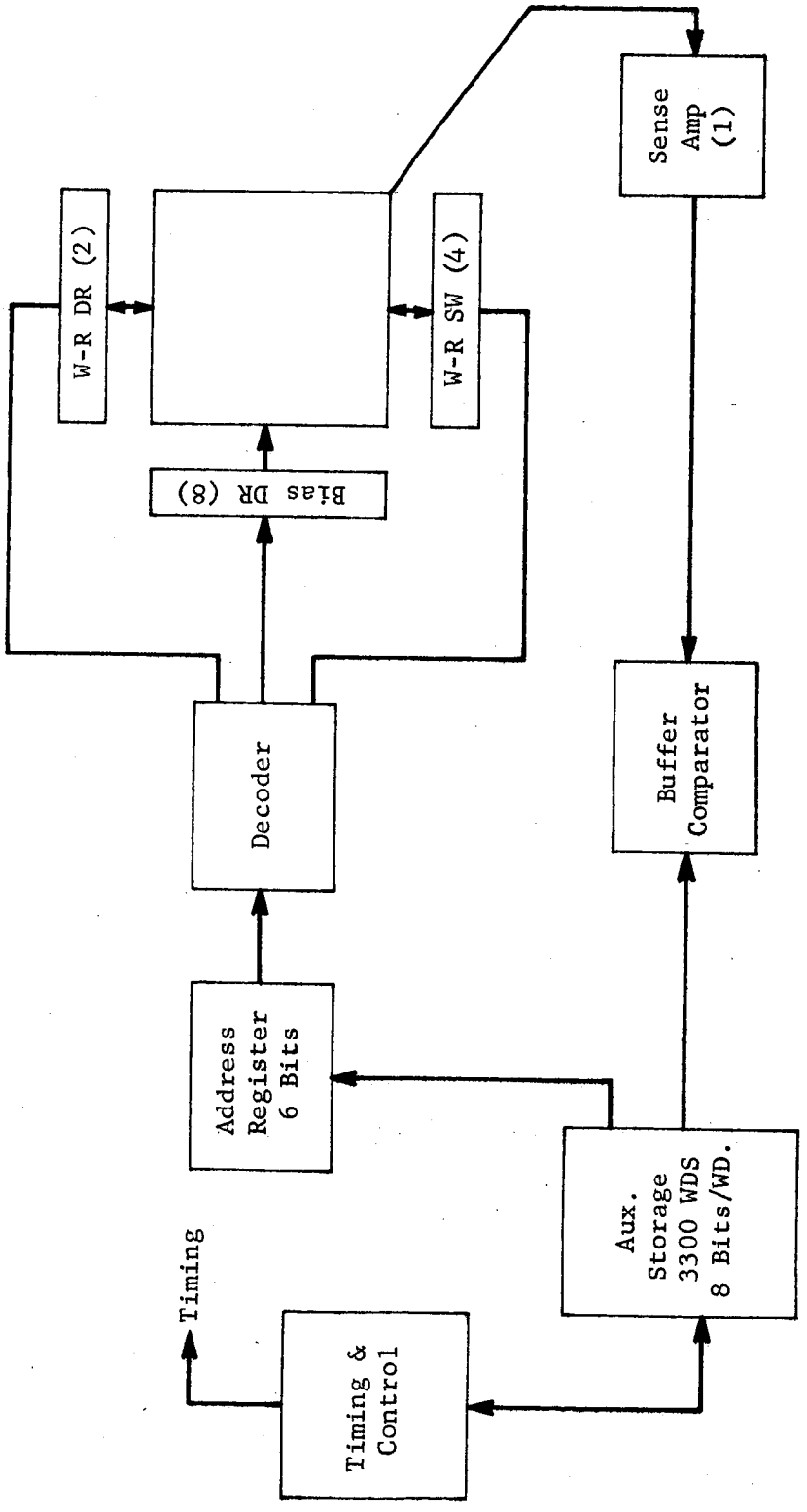


FIGURE 5.6 SYSTEM BLOCK DIAGRAM

126

by the address register content. After the 64 locations are read, the operator removes the card and another term is threaded. The process is repeated until all terms are threaded and tested.

5.1.2.7 Typical Circuit and Component Count: A typical circuit and component count for a tape reader system will be presented to evaluate the cost of the production test equipment.

The following list of circuits is representative of a typical system. The actual number of circuits and components will depend upon the type of storage utilized and the type of logic considered for the equipment.

Circuit	Quantity	
Address register flip-flops	6	
Data register flip-flops	4	(2 for input data and 2 for sense amplifier data)
Error flip-flop	1	
Address decoder	1	
Bias drivers	8	
Write/read drivers	2	
Write/read switches	4	
Sense amplifier	1	
Comparitor gates	2	
Comparitor amplifier	1	
Manual clock	1	
Timing generators (single-shot)	6	
Clock or gate	1	

An estimate for a component count will be given for transistors and diodes only. Commerical grade resistors and capacitors will be adequate and are relatively inexpensive.

Circuit	Transistors/cir	Diodes/cir	Total Transistors	Total Diodes
Address register	2	12	12	72
Data register	2	12	8	48
Error flip-flop	2	2	2	2
Address decoder				32
Bias drivers	3	2	24	16
Write/read drivers	6	4	12	8
Write/read switches	3	6	12	24
Sense amplifier	12	6	12	6
Comparitor gates	1	6	2	12
Comparitor amplifier	1	1	1	1
Manual clock	4		4	
Timing generators	3	2	18	12
Tape buffers	1	1	8	8
Total			115	241

The production test equipment is not required to operate over a wide range of temperature and shock. Therefore, the transistor and diode cost may be minimized. There are a few critical areas where special-purpose transistors and diodes may be required. The output stage of the current drivers and the sense amplifier input stages are examples of these. However, in general, a transistor such as the 2N404 and a diode such as S669G will be sufficient in 95 percent of the applications.

5.2 Maintenance Test Equipment

The purpose of the Maintenance Test Equipment is to provide production and maintenance personnel with a means of acceptance testing the completed logic module for wiring correctness and proper operation.

5.2.1 Testing Method

The Maintenance Test Equipment will be utilized to test a completed logic module before and after encapsulation. Therefore, the equipment must have the capability

of simulating system data programs and detecting proper sense line output for these programs. The most favorable method of implementing these capabilities would be to activate all inhibit terms in a logic matrix with the exception of those terms which thread the core under test. The enabled core would be subjected to a write/read current program and the sense line output viewed with an oscilloscope or detected with a calibrated sense amplifier. The remaining inhibit terms are activated individually and the sense line output tested for the proper inhibited output. The process is repeated until each core in a logic matrix has been tested.

An alternate method of testing, which would reduce the number of inhibit drivers required in the test equipment, is to activate only those inhibit terms which will inhibit all cores in the matrix except the core under test. This information would be available from the logic equations of the matrix under test. The remainder of the test procedure would be indentical to the above test. Either method of testing may be performed manually or fully automated with the logic routine contrained in some form of auxiliary storage.

5.2.2 Test Equipment Implementation

5.2.2.1 Selection Technique: Three types of current drivers (inhibit, write, and read) are required to test a completed logic module. Interconnection of these drivers to the module may be accomplished with the aid of a test fixture designed to accommodate the module terminals. The number of inhibit drivers required is variable and will depend upon the method of testing selected. A further reduction in the number of drivers required is possible providing inhibit terms are connected in series. However, the series connection of terms will reduce the matrix programming to a manual operation through use of switches and/or patch cords due to the prohibitive cost of electronic interconnections. The complexity of the inhibit driver circuit will be a function of the interconnection system selected.

The write and read drivers utilized in the test equipment are similar to the system drivers. The amplitude, pulse width, and rise and fall times should be variable to perform marginal checks. In the present system, P-time pulses are utilized as inhibit terms and write/read clocks. A P-time pulse generated coincidently with

the logic write clock time may function as an inhibit term through a portion of a logic matrix and as a write clock term through the remainder of the matrix. At present each core threaded by a P-time write clock is also linked by a P-time read clock. The P-time read clocks can be eliminated and only one system read clock utilized for all cores in the system. The elimination of the P-time read clocks would reduce the total number of wires and interconnections in the system and simplify the test procedure somewhat. The P-time write clocks still present a problem during testing in that the inhibit drivers must also function as a write clock. Therefore, if a single system read clock is utilized, only one read clock and one write clock driver will be required. The number of inhibit drivers required will be variable. Some of these drivers will be required to function as write clock drivers.

5.2.2.2 Sense Line Output: The output of the sense line may be viewed with an oscilloscope or a sense amplifier flip-flop system may be utilized as a go/no-go indicator. If the former method is selected, a graticule on which the minimum acceptable "one" and maximum "zero" waveforms are inscribed may be utilized as a test aid. If the go/no-go indicator is selected, the sense amplifier may be calibrated to the worst-case pattern. The output of the flip-flop would drive an indicator light registering an accept or reject situation. A polarity detecting feature may be incorporated into the sense amplifier section to verify proper sense line routing.

5.2.2.3 Timing Generator: The number of timing pulses required will be dependent upon the selected sensing system and the amount of automatic test features designed into the equipment. Certain basic pulses such as a test clock, inhibit driver clock, and a write and read clock will be required. These timing pulses may be easily derived utilizing standard design techniques.

5.2.2.4 Inhibit Driver Programming: In Paragraph 5.1.1 two methods of programming the inhibit drivers were discussed:

1) where all inhibit terms are activated with the exception of those terms threading the core under test

2) where only those inhibit terms necessary to inhibit all cores except the core under test are activated.

If 1) is selected, the logic lists may be utilized directly. If 2) is selected, an inhibit driver program list must be written noting which terms must be activated to prohibit switching of all the cores in the matrix with the exception of the core under test. An inspection of the logic lists will reveal this information and the required number of inhibit drivers will be reduced considerably. Connection of inhibit terms in series will further reduce the driver count. A manual system of interconnection utilizing jumper cords is considered adequate since the number of systems presently contemplated for production is small.

The inhibit driver programming will be further simplified for the equipment operator if the input and output terminals of all logic modules are standardized. A term would be assigned to the same terminal for every module in the system resulting in fewer interconnection changes and less confusion for the operator.

5.2.2.5 System Operation: A typical block diagram of a manual test system is shown in Figure 5.7. An automated test system is possible. However, for a small system such as the one under consideration, the cost of automating the process is prohibitive. If large scale production is contemplated, further consideration should be given to the fully automated tester.

For the manual system described the operator places a completed logic module in the test fixture and connects the proper inhibit driver output lines with jumper cords. Specific drivers are enabled as noted on the acceptance test sheet, and the matrix is subjected to a current pulse program identical to that in the final system. The output of the sense line is monitored either visually or with a sense amplifier. If the test indicates proper core performance, the succeeding core in the matrix is tested. The inhibit drivers listed for this core are enabled and the test is repeated until all cores in the matrix have been tested. Cores indicating less than average performance are retested to a marginal test program.

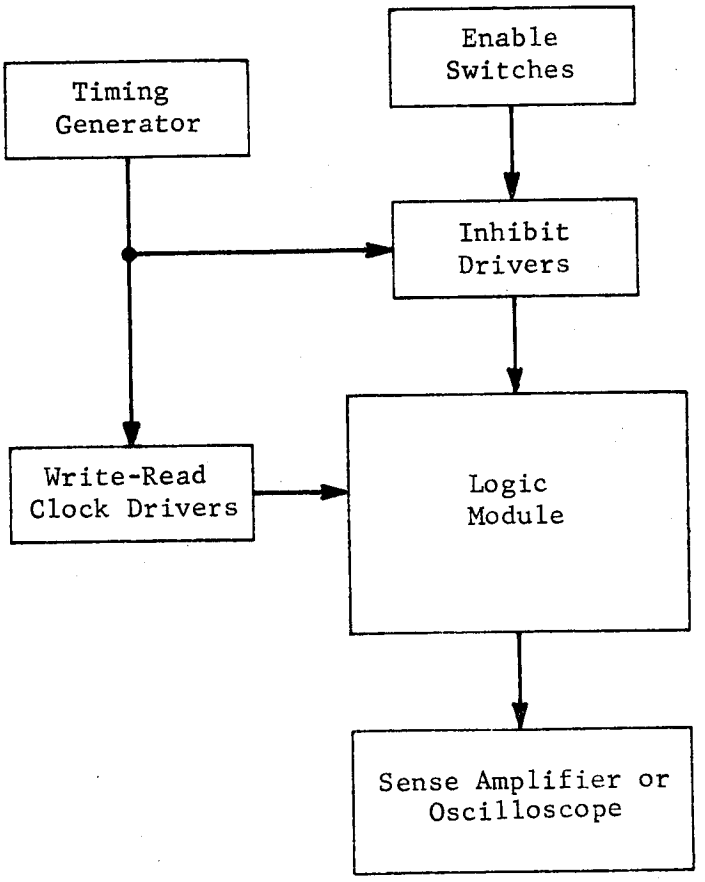


FIGURE 5.7 TEST SYSTEM BLOCK DIAGRAM

5.2.2.6 Component Count and Cost Estimate: The total number of components and cost of the test equipment will depend upon the selection of the test method and sensing system. The circuits described will not be required to meet adverse environment specifications and costs will be nominal. The same circuits used in the production tester will be adequate for most of the requirements of the module tester.

APPENDIX A

JPL LOGIC MEMORY CURRENT SPECIFICATION

Logic Write Clock Current Pulse

Amplitude I = 600 ma ± 5%
Pulse Width, tw = 2 μsec ± 10%
Rise Time t_R = 0.5 to 0.6 μsec (linear) - 0.55 nom.
Fall Time t_F = 0.1 to 0.2 μsec (linear) - 0.15 nom.

Rise and fall time are considered to be linear.

The logic read clock current pulse is specified identically to the logic write clock.

The start of the rise of the logic read pulse will be 50 μs from the start of the rise of the logic write pulse.

Inhibit Current Pulse

Amplitude I = 600 ma ±5%
Maximum pulse width = 4 μsec
Minimum pulse width = the 10% point of the rise of the inhibit pulse shall be within the 0 and 10% points of the rise of the write pulse; the 90% point of the fall of the inhibit pulse shall occur no earlier than the 90% point of the fall of the write pulse

Rise Time, $t_R \leq 0.5$ μsec (linear)
Fall Time, $t_F = \geq 0.2$ μsec (linear)

Pulse overshoot and droop are contained within the amplitude tolerances. Trailing edge undershoot is considered to be zero.

The ambient temperature range extends from -10° C to +85° C.

LIST OF SYMBOLS

H	-	Magnetic field intensity
H_O	-	Core Switching threshold field intensity
I	-	Drive current amplitude
I_i	-	Inhibit current pulse
I_{min}	-	Minimum drive current as specified by the JPL Current Specification
I_{max}	-	Maximum drive current as specified by the JPL Current Specification
I_{nom}	-	Nominal drive current as specified by the JPL Current Specification
I_R	-	Read current pulse
I_{RS}	-	Reset current pulse
I_S	-	Set current pulse
I_W	-	Write current pulse
S_W	-	Switching coefficient
T	-	Temperature in degrees centigrade
t_D	-	Delay time; time from t_o to the 10% point of uV_1 (See Figure A.1)
t_F	-	Fall time of drive current pulse from 90% to 10% of I.
t_o	-	Reference time, start of rise of read current pulse
t_P	-	Peaking time of uV_Z measured from t_o
T_P	-	Peaking time of uV_1 measured from t_o
t_R	-	Rise time of drive current pulse from 10% to 90% of I
T_S	-	Switching time of uV_1 measured across the 10% points of uV_1
T_{TS}	-	Total switching time of uV_1 from t_o to the 10% point of fall of uV_1 or $T_{TS} = t_D + T_S$
t_W	-	Drive current pulse width measured at start of rise to end of fall of current pulse
uV_1	-	Peak output voltage developed when a read current pulse is applied to a core in the "one" state
uV_Z	-	Peak output voltage developed when a read current pulse is applied to a core in the "zero" state.
V_F	-	Peak output voltage developed by the core due to fall of read current pulse
V_Z	-	Delta noise, voltage differential of uV_Z signals
V_{OL}	-	Zero output of the logic matrix
V_{1L}	-	One output of the logic matrix

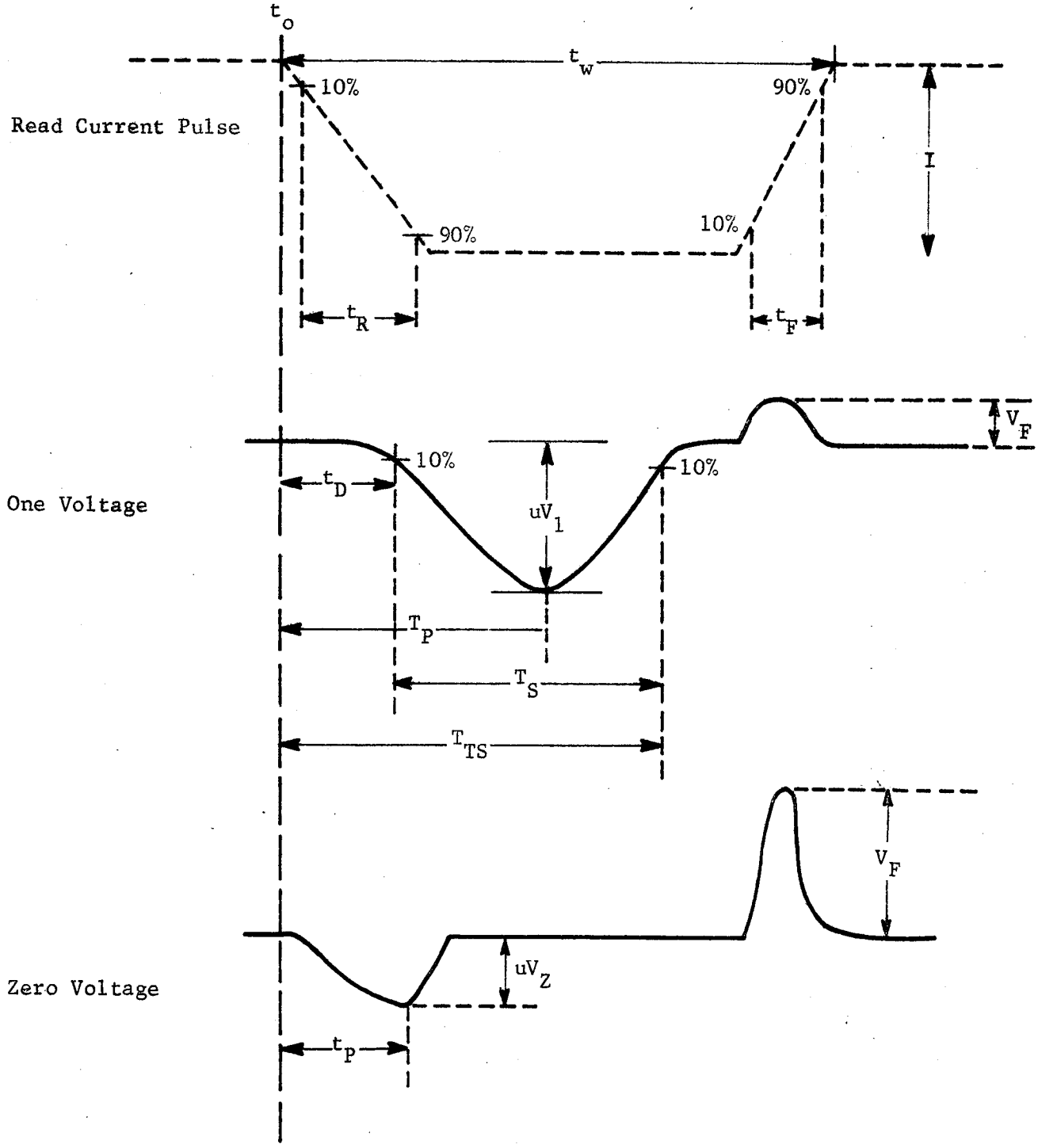


FIGURE A-1 DELAY TIME

Selection of Control Sample

Purpose

The purpose of this test is to select from the 91 EMI 81-104 cores and the 50 Lockheed 80-04 cores those units which exhibit the minimum and maximum switching parameters of uV_1 and uV_2. These min - max units will be designated as the control sample. All succeeding tests will then be performed on the control sample only. This will reduce the total amount of testing time for the study.

Test Conditions

The current program utilized in this test is shown in Figure A.2. A block diagram of the test equipment utilized in the test is shown in Figure A.3. A schematic of the current driver utilized to synthesize the current pulses is shown in Figure A.4. The current program for the test is as follows:

$$I_R = I_W \qquad I_i = 0$$

Current Pulse Specifications:

$I = 600$ ma
$t_R = 0.55\ \mu$sec
$t_F = 0.15\ \mu$sec
$t_W = 2.0\ \mu$sec

The following parameters were utilized as criteria in the selection of the control sample:

uV_1 - min-max
uV_2 - min-max
V_F - min-max
t_D - min-max
t_P - min-max
T_P - min-max
T_S - min-max

The test was conducted at 25° C.

Test Results

The results of this test are shown in Table A.1. Cores A-1, C-14 and E-11 of the EMI lot are selected as control samples. Cores 1, 14, 44 and 50 of the Lockheed lot are designated as the control sample. These cores will be identified as A through G respectively for the remainder of the succeeding tests.

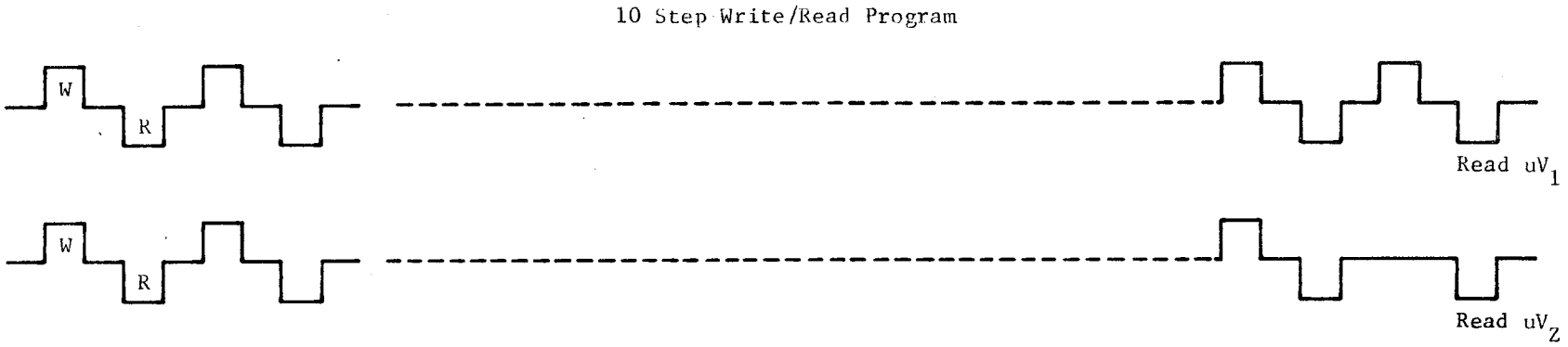


FIGURE A.3 CURRENT PROGRAM FOR SELECTION OF CENTRAL SAMPLE

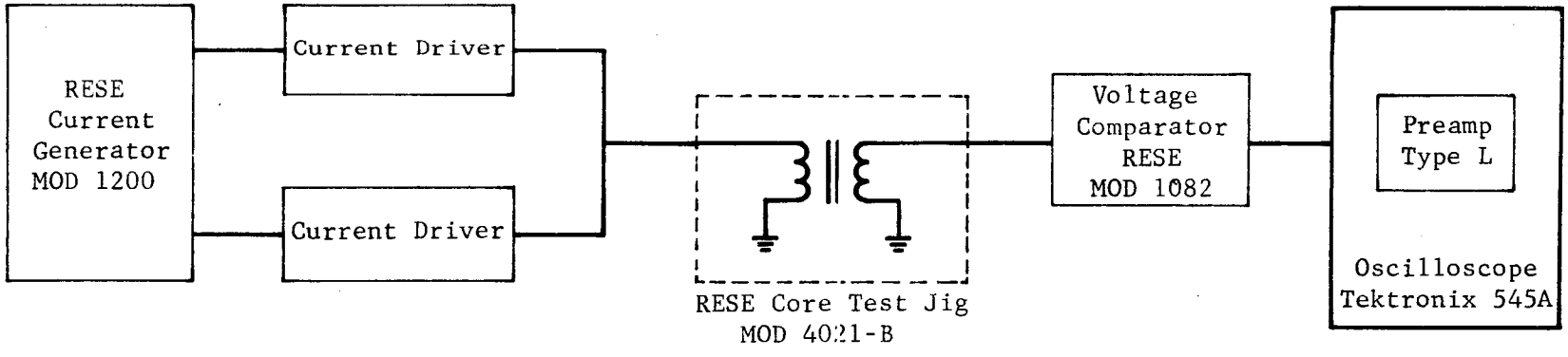


FIGURE A.3 BLOCK DIAGRAM OF TEST EQUIPMENT UTILIZED FOR SELECTION OF CONTROL SAMPLES

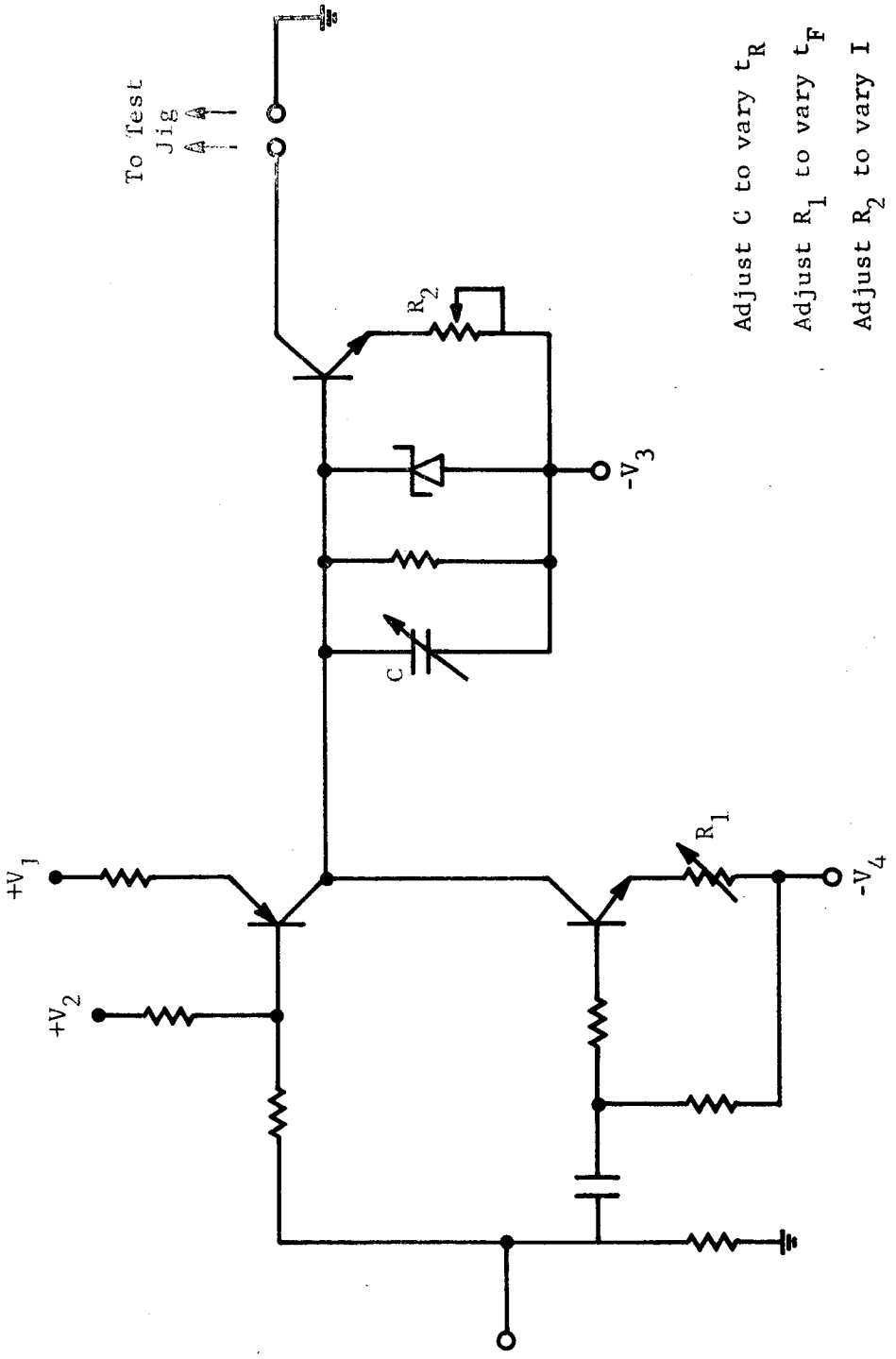


FIGURE 2.4 CURRENT DRIVER SCHEMATIC

The variations of the switching parameters of the two cores lots are summarized below:

Cores	uV_1	T_P	T_S	uV_Z
EMI 81-104	185-204 mv	0.87-0.93 μs	0.94-1.00 μs	2.92-3.21 mv
Lockheed 80-04	191-206 mv	0.84-0.86 μs	0.87-0.90 μs	2.98-3.30 mv

V_F
10.1-12.1 mv
10.5-12.1 mv

The switching parameters of the control sample are indicated below:
(Measured with the current program as above)

Core	uV_1	T_P	T_S	T_D	T_{TS}	uV_Z	t_P	V_F
A	204 mv	0.85 μs	0.94 μs	0.43 μs	1.37 μs	3.12 mv	0.74 μs	10.9 mv
B	186 mv	0.88 μs	0.99 μs	0.42 μs	1.41 μs	2.90 mv	0.73 μs	10.3 mv
C	189 mv	0.91 μs	0.97 μs	0.45 μs	1.42 μs	2.93 mv	0.73 μs	10.5 mv
D	192 mv	0.84 μs	0.94 μs	0.42 μs	1.36 μs	3.10 mv	0.73 μs	10.9 mv
E	191 mv	0.82 μs	0.90 μs	0.42 μs	1.32 μs	3.20 mv	0.74 μs	11.5 mv
F	196 mv	0.80 μs	0.89 μs	0.41 μs	1.30 μs	3.21 mv	0.72 μs	11.5 mv
G	205 mv	0.82 μs	0.91 μs	0.42 μs	1.33 μs	3.19 mv	0.72 μs	11.2 mv

TABLE A.1 uV_1 AND uV_Z MEASUREMENTS

TEST CONDITIONS: $I_R = I_W$ = NOMINAL TEMP $\approx$ 25° C

Core Type & Number	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_Z (mv)	t_P (μsec)	V_F (mv)
80-104 A-1	204	0.43	0.85	0.94	1.37	3.12	0 74	10.9
80-104 A-2	199	0.43	0.85	0.95	1.38	3.09	0.74	10.8
80-104 A-3	198	0.43	0.87	0.97	1.40	2.96	0.74	10.9
80-104 A-4	203	0.43	0.85	0.95	1.38	3.00	0.74	10.6
80-104 A-5	201	0.43	0.85	0.95	1.38	3.12	0.74	11.0
80-104 A-6	202	0.43	0.86	0.95	1.38	3.09	0.74	10.8
80-104 A-7	203	0.43	0.85	0.95	1.38	3.00	0.74	10.6
80-104 A-8	197	0.43	0.85	0.95	1.38	3.01	0.74	10.4
80-104 A-9	198	0.43	0.85	0.95	1.38	2.93	0.74	10.2
80-104 A-10	195	0.43	0.86	0.96	1.39	2.95	0.74	10.5
80-104 A-11	199	0.43	0.85	0.95	1.38	2.99	0.74	10.6
80-104 A-12	202	0.43	0.86	0.95	1.38	3.03	0.74	10.7
80-104 A-13	199	0.43	0.86	0.95	1.38	3.09	0.74	10.6
80-104 A-14	200	0.43	0.86	0.95	1.38	3.10	0.74	10.9
80-104 A-15	201	0.43	0.86	0.95	1.38	3.06	0.74	10.7
80-104 A-16	196	0.43	0.86	0.95	1.38	3.01	0.74	10.7
80-104 A-17	205	0.43	0.86	0.95	1.38	3.10	0.74	10.7
80-104 A-18	204	0.43	0.85	0.95	1.38	3.11	0.74	10.8
80-104 A-19	203	0.43	0.85	0.95	1.38	3.01	0.74	10.4
80-104 A-20	197	0.43	0.85	0.95	1.38	3.05	0.73	10.6
80-104 B-1	190	0.44	0.91	0.99	1.43	3.20	0.70	12.5
80-104 B-2	190	0.44	0.91	0.98	1.42	3.10	0.70	12.7
80-104 B-3	187	0.44	0.91	0.97	1.41	3.04	0.70	11.9
80-104 B-4	187	0.44	0.91	0.99	1.43	3.16	0.70	11.8
80-104 B-5	189	0.44	0.91	0.98	1.42	3.03	0.70	12.0
80-104 B-6	185	0.44	0.91	0.98	1.42	2.90	0.70	11.8

TABLE A.1 uV_1 AND uV_Z MEASUREMENTS (Continued)

Core Type & Number	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_Z (mv)	t_P (μsec)	V_F (mv)
80-104 B-7	190	0.44	0.91	0.99	1.43	3.03	0.70	11.9
80-104 B-8	192	0.44	0.90	0.98	1.42	3.08	0.70	12.0
80-104 B-9	191	0.44	0.91	0.99	1.43	3.14	0.70	12.7
80-104 B-10	187	0.44	0.92	0.97	1.41	2.92	0.70	11.9
80-104 B-11	186	0.44	0.92	0.98	1.42	3.01	0.70	11.7
80-104 B-12	186	0.44	0.91	0.98	1.42	2.94	0.70	11.9
80-104 B-13	186	0.44	0.92	0.98	1.42	2.97	0.70	12.0
80-104 B-14	186	0.44	0.91	0.98	1.42	2.98	0.70	12.1
80-104 B-15	187	0.44	0.91	0.97	1.41	2.90	0.70	12.0
80-104 B-16	191	0.44	0.91	0.97	1.41	3.02	0.70	11.8
80-104 B-17	188	0.44	0.91	0.99	1.43	3.19	0.70	12.5
80-104 B-18	190	0.44	0.91	0.98	1.42	3.11	0.70	12.3
80-104 B-19	190	0.44	0.91	0.98	1.42	3.17	0.70	12.1
80-104 B-20	187	0.44	0.91	0.97	1.43	3.07	0.70	12.1
80-104 C-1	190	0.43	0.89	0.97	1.40	2.91	0.74	10.5
80-104 C-2	195	0.43	0.88	0.96	1.39	3.03	0.74	10.8
80-104 C-3	192	0.43	0.88	0.96	1.39	3.06	0.74	11.1
80-104 C-4	191	0.43	0.89	0.96	1.39	2.98	0.73	10.4
80-104 C-5	191	0.43	0.88	0.96	1.39	3.16	0.74	11.2
80-104 C-6	193	0.44	0.89	0.96	1.40	3.03	0.73	10.4
80-104 C-7	194	0.43	0.89	0.96	1.39	3.03	0.73	10.7
80-104 C-8	189	0.43	0.89	0.98	1.41	3.00	0.73	10.7
80-104 C-9	192	0.44	0.89	0.97	1.41	2.92	0.73	10.3
80-104 C-10	194	0.43	0.89	0.97	1.40	2.97	0.73	10.5
80-104 C-11	192	0.43	0.88	0.97	1.40	3.11	0.73	11.0
80-104 C-12	192	0.43	0.89	0.96	1.39	3.11	0.73	11.0
80-104 C-13	190	0.43	0.89	0.97	1.40	2.90	0.73	10.3
80-104 C-14	186	0.42	0.88	0.99	1.41	3.11	0.73	11.0

TABLE A.1 uV_1 AND uV_Z MEASUREMENTS (Continued)

Core Type & Number	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_Z (mv)	t_P (μsec)	V_F (mv)
80-104 C-15	192	0.43	0.88	0.96	1.39	3.03	0.73	10.9
80-104 C-16	192	0.44	0.89	0.96	1.40	3.08	0.73	10.8
80-104 C-17	192	0.43	0.89	0.96	1.39	3.08	0.73	10.9
80-104 C-18	192	0.43	0.89	0.96	1.39	2.96	0.73	10.4
80-104 C-19	193	0.43	0.89	0.96	1.39	3.02	0.73	10.6
80-104 C-20	194	0.43	0.88	0.96	1.39	3.06	0.72	10.9
80-104 D-1	186	0.40	0.87	0.98	1.38	3.10	0.70	10.9
80-104 D-2	187	0.40	0.87	0.97	1.37	3.12	0.70	11.1
80-104 D-3	190	0.40	0.87	0.98	1.38	3.13	0.70	11.1
80-104 D-4	187	0.40	0.88	0.98	1.38	3.13	0.69	11.0
80-104 D-5	186	0.40	0.88	0.98	1.38	3.12	0.69	10.8
80-104 D-6	186	0.40	0.87	0.98	1.38	2.98	0.70	10.3
80-104 D-7	186	0.40	0.87	0.98	1.38	3.13	0.69	11.0
80-104 D-8	188	0.40	0.87	0.98	1.38	3.17	0.69	11.0
80-104 D-9	187	0.41	0.87	0.99	1.40	3.10	0.69	10.9
80-104 D-10	187	0.40	0.88	0.98	1.38	3.07	0.70	10.6
80-104 D-11	190	0.40	0.88	0.98	1.38	3.11	0.70	11.0
80-104 D-12	186	0.39	0.87	0.98	1.37	3.22	0.70	11.3
80-104 D-13	188	0.41	0.87	0.99	1.40	2.96	0.70	10.4
80-104 D-14	191	0.40	0.87	0.98	1.38	2.93	0.70	10.3
80-104 D-15	190	0.41	0.88	0.99	1.40	3.10	0.70	10.9
80-104 D-16	189	0.40	0.87	0.97	1.37	3.08	0.69	10.8
80-104 D-17	187	0.41	0.88	0.99	1.40	3.02	0.69	10.5
80-104 D-18	184	0.40	0.88	0.98	1.38	3.05	0.70	10.7
80-104 D-19	191	0.41	0.87	0.98	1.39	3.00	0.70	10.5
80-104 D-20	192	0.40	0.88	0.98	1.38	3.10	0.70	11.3

TABLE A.1 uV_1 AND uV_Z MEASUREMENTS (Continued)

Core Type & Number	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_Z (mv)	t_P (μsec)	V_F (mv)
80-104 E-1	192	0.43	0.90	0.99	1.42	3.09	0.74	11.1
80-104 E-2	191	0.44	0.90	0.98	1.42	2.98	0.74	10.6
80-104 E-3	191	0.43	0.90	0.99	1.42	3.08	0.74	10.8
80-104 E-4	191	0.44	0.90	0.98	1.42	2.95	0.74	10.3
80-104 E-5	191	0.44	0.90	0.98	1.42	2.95	0.74	10.5
80-104 E-6	194	0.44	0.89	0.97	1.41	2.99	0.74	10.8
80-104 E-7	192	0.43	0.90	0.99	1.42	3.14	0.74	11.0
80-104 E-8	194	0.43	0.89	0.98	1.41	3.08	0.74	11.3
80-104 E-9	195	0.44	0.89	0.97	1.41	3.05	0.73	10.9
80-104 E-10	193	0.44	0.90	0.98	1.42	2.93	0.73	10.5
80-104 E-11	189	0.45	0.91	0.97	1.42	2.93	0.73	10.5
80-04 1	192	0.42	0.84	0.94	1.36	3.10	0.73	10.9
80-04 2	200	0.42	0.80	0.89	1.31	3.35	0.74	11.5
80-04 3	200	0.42	0.84	0.90	1.32	3.24	0.73	11.3
80-04 4	197	0.42	0.81	0.90	1.32	3.32	0.74	12.0
80-04 5	195	0.42	0.82	0.90	1.32	3.18	0.74	11.4
80-04 6	205	0.42	0.81	0.90	1.32	3.16	0.73	11.2
80-04 7	195	0.42	0.81	0.89	1.31	3.29	0.73	11.7
80-04 8	196	0.42	0.82	0.90	1.30	3.22	0.74	11.5
80-04 9	200	0.42	0.81	0.91	1.33	3.23	0.74	11.2
80-04 10	196	0.42	0.82	0.90	1.32	3.33	0.74	11.7
80-04 11	193	0.42	0.82	0.91	1.33	3.32	0.74	11.9
80-04 12	202	0.42	0.81	0.89	1.31	3.36	0.74	12.0
80-04 13	195	0.42	0.80	0.88	1.30	3.20	0.74	11.4
80-04 14	191	0.42	0.82	0.90	1.32	3.20	0.74	11.5
80-04 15	193	0.42	0.80	0.89	1.31	3.24	0.74	11.6
80-04 16	206	0.42	0.80	0.90	1.32	3.17	0.74	11.4
80-04 17	199	0.42	0.80	0.90	1.32	3.22	0.74	11.5

TABLE A.1 uV_1 AND uV_Z MEASUREMENTS (Continued)

Core Type & Number	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_Z (mv)	t_P (μsec)	V_F (mv)
80-04 18	197	0.42	0.81	0.90	1.32	3.25	0.74	11.8
80-04 19	198	0.42	0.80	0.89	1.31	3.13	0.74	11.0
80-04 20	196	0.42	0.81	0.90	1.32	3.17	0.74	11.3
80-04 21	203	0.42	0.81	0.91	1.33	3.23	0.73	11.4
80-04 22	196	0.42	0.81	0.91	1.33	3.27	0.73	11.5
80-04 23	202	0.42	0.80	0.89	1.31	3.28	0.73	11.4
80-04 24	193	0.42	0.84	0.91	1.33	3.22	0.73	11.5
80-04 25	198	0.42	0.84	0.90	1.32	3.18	0.73	11.2
80-04 26	200	0.42	0.80	0.89	1.31	3.40	0.72	12.0
80-04 27	206	0.43	0.81	0.90	1.33	3.24	0.72	11.5
80-04 28	201	0.43	0.85	0.90	1.33	3.17	0.72	11.3
80-04 29	200	0.43	0.83	0.89	0.32	3.29	0.72	11.5
80-04 30	192	0.42	0.82	0.90	1.32	3.21	0.72	11.4
80-04 31	201	0.43	0.81	0.89	1.32	3.20	0.72	11.3
80-04 32	205	0.43	0.81	0.90	1.33	3.21	0.72	11.2
80-04 33	200	0.43	0.81	0.89	1.32	3.33	0.72	11.6
80-04 34	196	0.43	0.83	0.90	1.33	3.23	0.72	11.4
80-04 35	201	0.43	0.81	0.89	1.32	3.25	0.72	11.1
80-04 36	200	0.43	0.83	0.89	1.32	3.30	0.72	11.6
80-04 37	202	0.43	0.81	0.89	1.32	3.21	0.72	11.1
80-04 38	194	0.43	0.83	0.90	1.33	3.10	0.72	11.0
80-04 39	200	0.42	0.81	0.90	1.32	3.21	0.72	11.1
80-04 40	201	0.43	0.80	0.89	1.32	3.27	0.72	11.7
80-04 41	193	0.41	0.80	0.89	1.30	3.38	0.72	11.8
80-04 42	202	0.42	0.80	0.88	1.30	3.25	0.72	11.3
80-04 43	197	0.42	0.82	0.90	1.32	3.19	0.72	11.1
80-04 44	196	0.41	0.80	0.90	1.31	3.21	0.72	11.5
80-04 45	200	0.42	0.80	0.90	1.32	3.11	0.72	10.8

TABLE A.1 uV_1 AND uV_Z MEASUREMENTS (Continued)

Core Type & Number	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_Z (mv)	t_P (μsec)	V_F (mv)
80-04 46	198	0.42	0.82	0.89	1.31	3.20	0.72	11.2
80-04 47	197	0.42	0.85	0.91	1.33	3.15	0.72	11.2
80-04 48	198	0.42	0.82	0.90	1.32	3.25	0.72	11.6
80-04 49	196	0.42	0.80	0.89	1.31	3.33	0.73	11.7
80-04 50	205	0.42	0.82	0.91	1.33	3.19	0.72	11.2

APPENDIX B

DETERMINATION OF VARIATION OF uV_1 and uV_Z

Purpose

The purpose of this test is to determine the variations of uV_1 and uV_Z for the control sample under a minimum charge program and a maximum charge program over the temperature range of -10° C to +85° C.

Test A Maximum Charge Program

The current program utilized in this test is shown in Figure B.1. Figures A.3 and A.4 of Appendix A are applicable for the test equipment setup and current driver schematic. The current program for this test is as follows:

Current Program: Maximum Charge

$$I_R = I_W \quad I_i = 0$$

$$I = 630 \text{ ma}$$

$$t_R = 0.5 \ \mu\text{sec}$$

$$t_F = 0.1 \ \mu\text{sec}$$

$$t_W = 2.2 \ \mu\text{sec}$$

The test was performed at -10° C, +25° C and +85° C. The following parameters were measured:

uV_1, T_P, T_S, t, T_{TS}

uV_{Z1}, uV_{Z2}, t_{P1}, t_{P2}, V_{F1}, V_{F2}

Test B Minimum Charge Program

Test B is identical to test A with the exception of the current program.

Current Program - Minimum Charge

$$I_R = I_W \qquad I_i = 0$$

FIGURE B.1 CURRENT PROGRAM TESTS (A) AND (B)

$I = 570$ ma

$t_R = 0.6$ μsec

$t_F = 0.2$ μsec

$t_W = 1.8$ μsec

The switching parameters noted in test (A) were measured during this test.

Test Results

The results of tests A and B are listed in Tables B.1 and B.2 respectively. uV_1 vs temperature is shown in Figure B.2 for cores C and E. At -10° C with the minimum charge current program cores A, B, and C (EMI control units) are not fully switching and all of the flux written into the core is not being read. This fact is corroborated in Figures B.3 and B.4 where uV_{Z1}, and uV_{Z2} are plotted for cores A and F. The following table summarizes the test data.

uV_1 Variations

Core Type	V_1 min mv	V_1 max mv	T_P min μs	T_P max μs	T_S min μs	T_S max μs	T_D min μs	T_D max μs	T_{TS} min μs	T_{TS} max μs
81-104	123	261	0.64	0.97	0.68	1.27*	0.22	0.42	0.98	1.49*
80-04	135	253	0.63	0.96	0.64	1.23*	0.26	0.42	0.94	1.49*

uV_Z Variations

Core Type	uV_{Z1} min mv	uV_{Z2} max mv	uV_{Z2} min mv	uV_{Z2} max mv	t_{P1} min μs	t_{P1} max μs	t_{P2} min μs	t_{P2} max μs	V_{F1} min mv	V_{F1} max mv	V_{F2} min mv	V_{F2} max mv
81-104	3.59	5.90	3.19	5.65	0.14	0.80	0.12	0.24	10.9	26.8	10.5	26.8
80-04	3.64	5.61	3.27	5.65	0.08	0.80	0.10	0.20	11.1	32.9	10.9	32.9

Total uV_1 and uV_Z variation with $I_R = I_W = I_{min} = I_{max}$

*Core not fully switching

TABLE B.1 uV_1 AND uV_Z MEASUREMENTS OF CONTROL SAMPLES

TEST CONDITION: $I_R = I_W$ = MAXIMUM CHARGE PROGRAM

Core No.	Temp °C	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{TS} (μsec)	uV_{Z1} (mv)	uV_{Z2} (mv)	t_{P1} (μsec)	t_{P2} (μsec)	V_{F1} (mv)	V_{F2} (mv)
	-10	188	0.34	0.86	1.11	1.45	4.28	4.09	0.14	0.14	25.7	25.7
A	+25	215	0.38	0.79	0.94	1.32	4.09	4.06	0.14	0.12	24.3	24.3
	+85	261	0.30	0.64	0.68	0.98	5.01	5.00	0.16	0.16	26.4	26.4
	-10	165	0.32	0.88	1.17	1.49	4.40	4.10	0.18	0.18	26.8	26.8
B	+25	196	0.39	0.82	0.98	1.37	4.06	3.90	0.14	0.14	24.4	24.3
	+85	255	0.34	0.68	0.68	1.02	4.87	4.78	0.14	0.14	26.1	26.1
	-10	168	0.33	0.89	1.16	1.49	4.29	4.08	0.22	0.20	26.4	26.4
C	+25	200	0.40	0.83	0.95	1.35	4.03	4.05	0.14	0.14	23.8	23.8
	+85	251	0.34	0.68	0.68	1.02	4.92	4.76	0.14	0.14	25.6	25.6
	-10	174	0.35	0.87	1.07	1.42	4.22	4.06	0.20	0.18	25.9	25.9
D	+25	208	0.38	0.77	0.88	1.26	5.61	5.65	0.08	0.10	32.9	32.9
	+85	248	0.30	0.63	0.65	0.95	5.28	5.20	0.14	0.14	28.0	28.0
	-10	172	0.35	0.87	1.06	1.41	4.24	4.15	0.16	0.16	26.6	26.6
E	+25	208	0.38	0.77	0.87	1.25	4.12	4.24	0.14	0.12	25.8	25.3
	+85	247	0.30	0.63	0.64	0.94	5.34	5.19	0.14	0.14	28.1	28.1
	-10	173	0.34	0.86	1.06	1.40	4.41	4.30	0.18	0.16	27.0	27.0
F	+25	208	0.37	0.77	0.88	1.25	4.34	4.30	0.14	0.12	25.5	25.5
	+85	247	0.29	0.63	0.65	0.94	5.37	5.22	0.14	0.14	28.2	28.2
	-10	175	0.35	0.86	1.07	1.40	4.42	4.26	0.22	0.20	27.3	27.3
G	+25	212	0.37	0.77	0.88	1.25	4.33	4.30	0.14	0.12	26.0	26.0
	+85	253	0.30	0.63	0.64	0.94	5.38	5.34	0.14	0.14	29.4	29.4

TABLE B.2 uV_1 AND uV_2 MEASUREMENTS OF CONTROL SAMPLES

TEST CONDITIONS: $I_R = I_W$ = MINIMUM CHARGE PROGRAM

Core No.	Temp °C	uV_1 (mv)	T_D (μsec)	T_P (μsec)	T_S (μsec)	T_{IS} (μsec)	uV_{Z1} (mv)	uV_{Z2} (mv)	t_{P1} (μsec)	t_{P2} (μsec)	V_{F1} (mv)	V_{F2} (mv)
	-10	152	0.26	0.96	1.23	1.49	5.90	3.85	0.80	0.22	13.0	12.5
A	+25	195	0.40	0.92	0.98	1.38	3.73	3.24	0.20	0.20	10.9	10.6
	+85	216	0.37	0.80	0.81	1.18	4.18	3.99	0.14	0.14	12.0	11.8
	-10	123	0.22	0.96	1.27	1.49	4.91	3.73	0.78	0.22	12.9	12.5
B	+25	173	0.38	0.96	1.05	1.43	3.59	3.19	0.20	0.20	10.9	10.5
	+85	210	0.40	0.83	0.77	1.21	3.95	3.72	0.14	0.14	11.3	11.3
	-10	125	0.23	0.97	1.26	1.49	5.30	3.78	0.78	0.24	13.0	12.7
C	+25	174	0.42	0.97	1.04	1.46	3.74	3.22	0.24	0.24	11.0	10.9
	+85	204	0.39	0.83	0.83	1.22	3.85	3.65	0.14	0.14	11.4	11.4
	-10	139	0.26	0.96	1.23	1.49	4.71	3.62	0.78	0.20	12.4	11.7
D	+25	182	0.42	0.91	0.95	1.37	3.64	3.27	0.20	0.20	11.1	10.9
	+85	201	0.33	0.75	0.80	1.13	4.20	3.96	0.14	0.14	11.9	11.9
	-10	135	0.26	0.96	1.23	1.49	4.57	3.68	0.80	0.20	12.5	12.1
E	+25	179	0.42	0.91	0.96	1.38	3.73	3.36	0.20	0.20	11.5	11.1
	+85	201	0.33	0.75	0.78	1.11	4.25	4.12	0.14	0.14	12.7	12.6
	-10	135	0.26	0.96	1.23	1.49	4.92	3.84	0.78	0.20	13.0	12.5
F	+25	180	0.42	0.91	0.96	1.38	3.80	3.43	0.20	0.20	11.8	11.5
	+85	201	0.33	0.75	0.78	1.11	4.31	4.16	0.14	0.14	12.7	12.3
	-10	138	0.27	0.96	1.22	1.49	4.54	3.73	0.78	0.20	12.5	12.3
G	+25	183	0.41	0.92	0.95	1.36	3.70	3.41	0.20	0.20	11.7	11.4
	+85	206	0.33	0.74	0.77	1.10	4.42	4.20	0.14	0.14	12.4	12.4

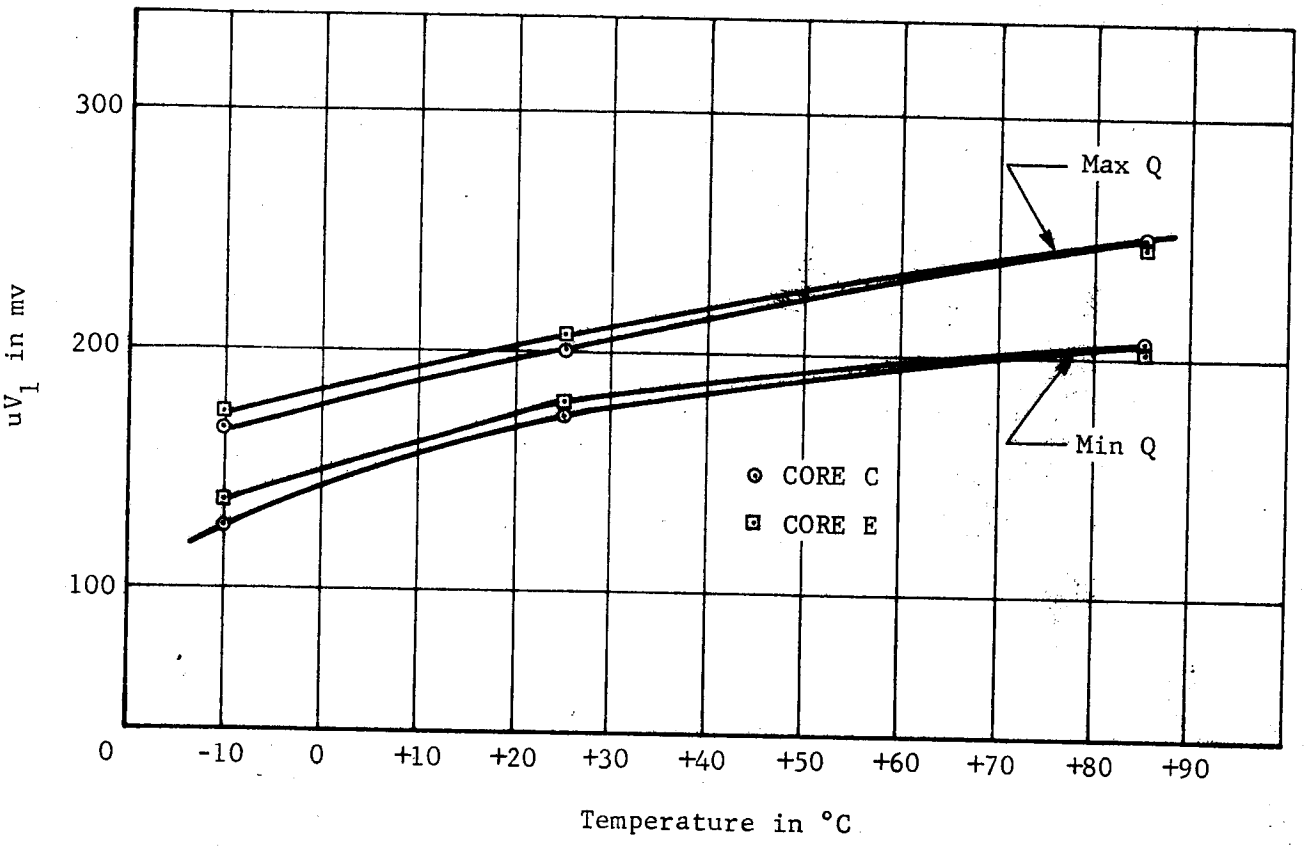


FIGURE B.2 uV_1 VS TEMPERATURE

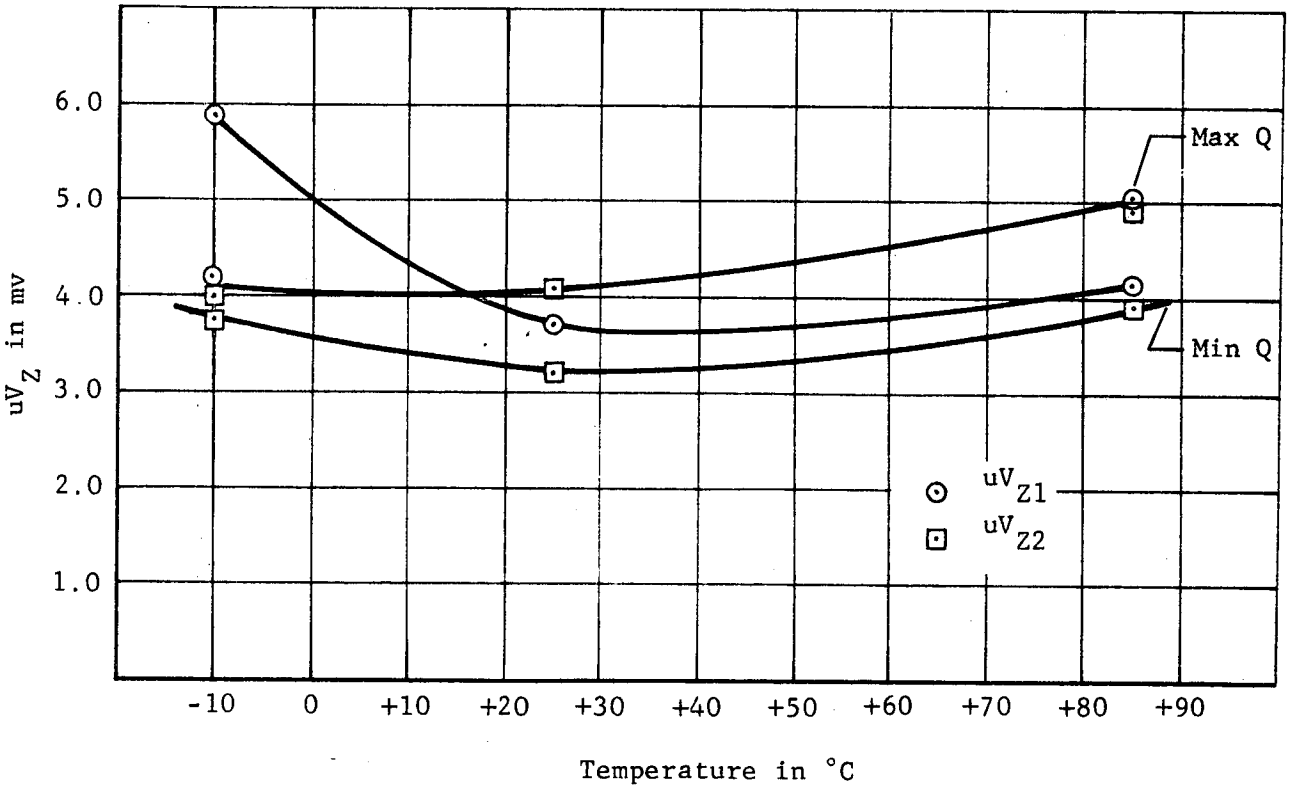


FIGURE B.3 uV_Z VS TEMPERATURE - CORE A

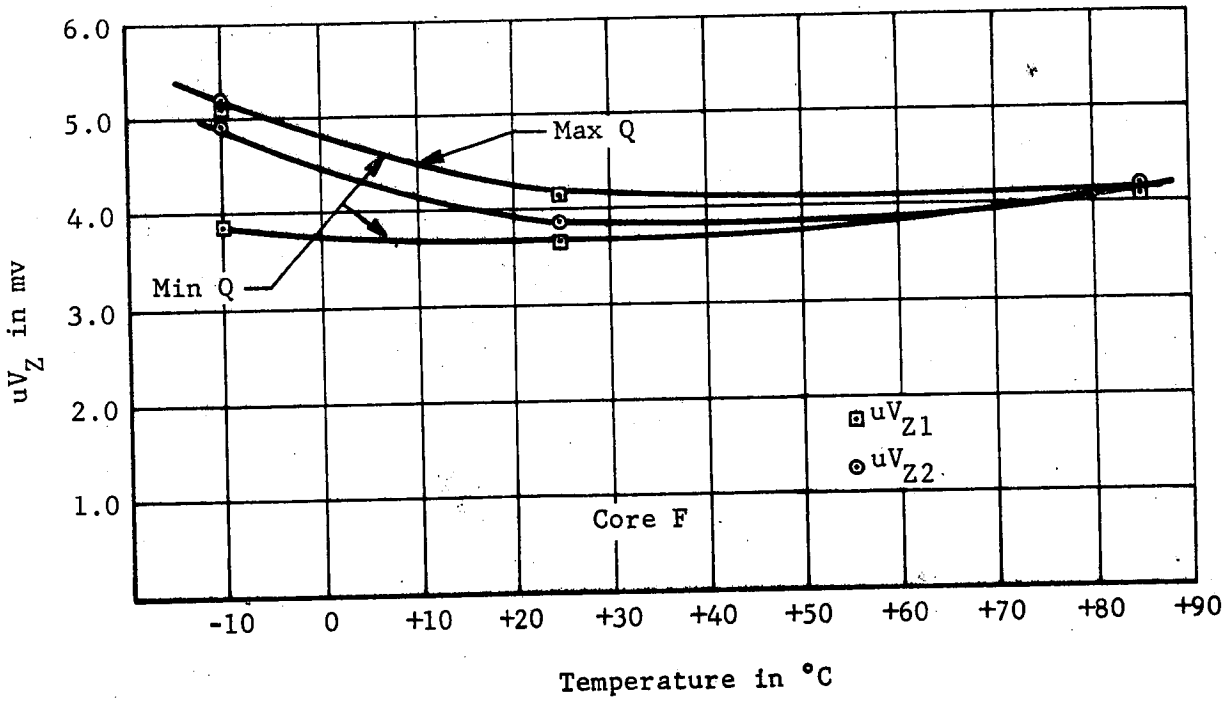


FIGURE B.4 uV_Z VS TEMPERATURE

APPENDIX C

INHIBIT CURRENT EFFECTS UPON THE SWITCHING PARAMETERS OF THE "ONE" SIGNAL

Purpose

The purpose of this test is to determine what effects the inhibit current pulse has upon the switching parameters of the "one" signal. The parameters to be measured are uV_1, and T_P. The tests will be conducted at -10° C and +85° C.

Test Conditions

Test (A) Maximum and Minimum Charge Program

The control sample was subjected to the minimum and maximum charge programs at -10° C and +85° C. uV_1 and T_P were measured.

Test (B) Minimum Charge Program with Inhibit Pulse

The current program utilized in this test is shown in Figure C.1. Figures A.3 and A.4 of Appendix A are applicable for the equipment setup with the exception that the inhibit pulse is derived from the third current generator in the Rise Pulse Generator. The test was conducted at -10° C and +85° C. uV_1 and T_P were recorded.

Test (C) Unbalanced Program with Inhibit Pulse

The current program utilized in this test is shown in Figure C.1. The control sample was subjected to the following current programs:

1) I_R = min Q I_W = max Q I_i = 2 amps t_W = 4 μsec

2) I_R = max Q I_W = min Q I_i = 2 amps t_W = 4 μsec

Test Results

The results of tests (A), (B), and (C) are shown in Tables C.1, C.2, and C.3. The switching parameters of uV_1 are extremely sensitive to the application of the inhibit pulse and the write/read current program. With I_W = max Q and I_R = min Q the cores are not fully read and flux is left in the core. Peaking time variations range from 0.73 to 1.26 μ sec. The minimum uV_1 observed for the tests was 0.065 volt.

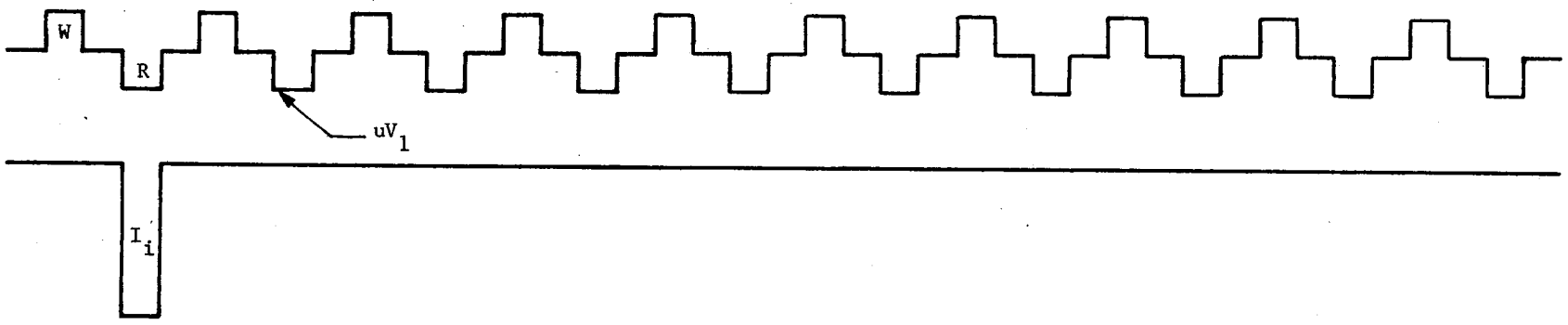


FIGURE C.1 CURRENT PROGRAM FOR TESTS A AND B

TABLE C.1 uV_1 MEASUREMENTS OF CONTROL SAMPLES

Test Conditions: $I_R = I_W$ = Minimim Charge Program

Inhibit Current		$I_i = 0$		$I_i = 2.00$ Amps	
Core No.	Temp °C	uV_1 (mv)	T_P (μsec)	uV_1 (mv)	T_P (μsec)
A	-10	138	1.00	098	0.92
	+85	224	0.84	222	0.86
B	-10	109	1.02	068	0.88
	+85	214	0.89	213	0.90
C	-10	113	0.99	065	0.88
	+85	208	0.90	208	0.91
D	-10	126	1.02	076	0.90
	+85	222	0.82	221	0.82
E	-10	121	1.03	076	0.90
	+85	222	0.82	221	0.82
F	-10	121	1.03	080	0.91
	+85	222	0.82	221	0.82
G	-10	124	1.03	080	0.91
	+85	228	0.82	228	0.82

TABLE C.2 uV_1 MEASUREMENTS OF CONTROL SAMPLES

Test Conditions: $I_R = I_W$ = Maximum Charge Program

Core No.	Temp °C	uV_1 (mv)	T_P (sec)
A	-10	184	0.91
	+85	268	0.70
B	-10	161	0.94
	+85	252	0.71
C	-10	162	0.96
	+85	247	0.72
D	-10	170	0.93
	+85	248	0.70
E	-10	166	0.93
	+85	257	0.68
F	-10	168	0.92
	+85	257	0.68
G	-10	171	0.92
	+85	263	0.68

TABLE C.3 uV_1 MEASUREMENTS OF CONTROL SAMPLES

Test Conditions		I_R = Minimum Charge I_W = Maximum Charge	I_i = 2.0 Amps	I_R = Max. Charge I_W = Min. Charge	I_i = 2.0 Amps
Core No.	Temp °C	uV_1 (mv)	T_P (μsec)	uV_1 (mv)	T_P (μsec)
A	-10	140	1.20	137	0.74
	+85	217	0.88	279	0.67
B	-10	117	1.24	100	0.73
	+85	206	0.90	264	0.70
C	-10	121	1.26	094	0.73
	+85	204	0.91	260	0.73
D	-10	126	1.22	114	0.73
	+85	217	0.82	274	0.66
E	-10	122	1.23	114	0.73
	+85	218	0.82	273	0.66
F	-10	124	1.23	114	0.73
	+85	220	0.82	274	0.66
G	-10	125	1.22	120	0.73
	+85	224	0.82	280	0.66

APPENDIX D

DETERMINATION OF VARIATIONS OF uV_1 AND T_p

Purpose

The purpose of this test is to determine the variations of uV_1 and T_p as a function of the inhibit current amplitude. The test was conducted at -10° C. Core C of the control sample was saluted as the worst-case device.

Test Conditions

Test A Minimum Charge Program with Inhibit Pulse

Core C was subjected to the minimum charge write/read program and the inhibit current amplitude was varied from 0 to 8.32 amp-turns. The current program is shown in Figure D.1. uV_1 and T_p were recorded.

Test B Min. Write-Max Read Charge Program with Inhibit uV_1 and T_p were recorded.

Test C Max. Write-Min Read Charge Program with Inhibit uV_1 and T_p were recorded.

Test Results

The results of tests A, B and C are shown in Table D.1. The peaking time, T_p, varied from 0.06 to 1.12 μsec over the range of the current program. The output amplitude at peaking time, uV_1, varied from 43.5 to 139 mv. Figures D.2, D.3 and D.4 show the variation of uV_1 as a function of I_i.

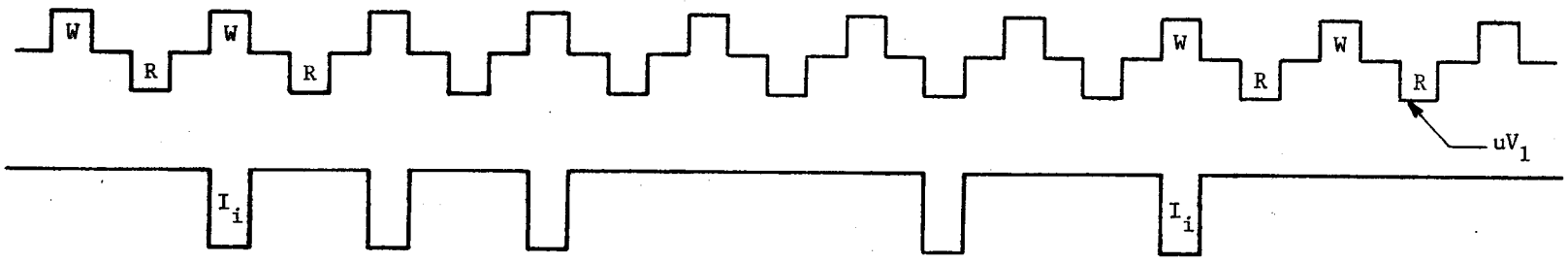


FIGURE D.1 uV_1 VS INHIBIT CURRENT PROGRAM

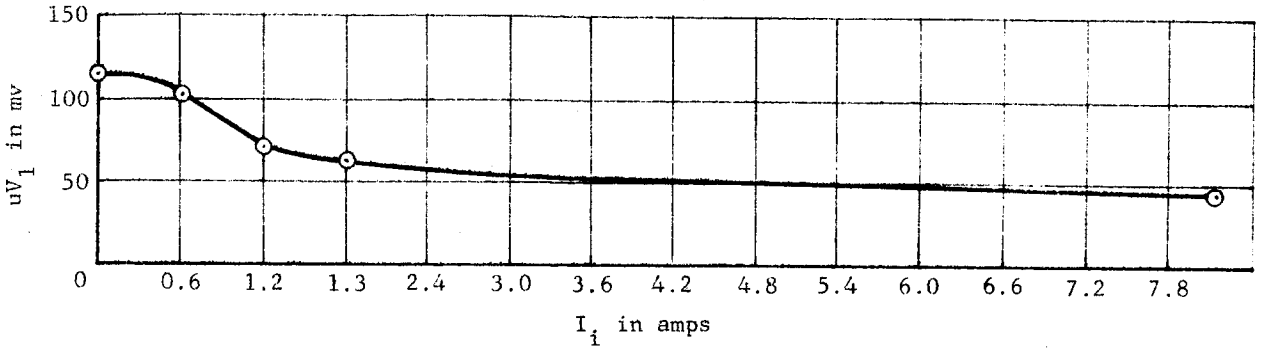


FIGURE D.2 uV_1 VS I_i MIN CHARGE PROGRAM

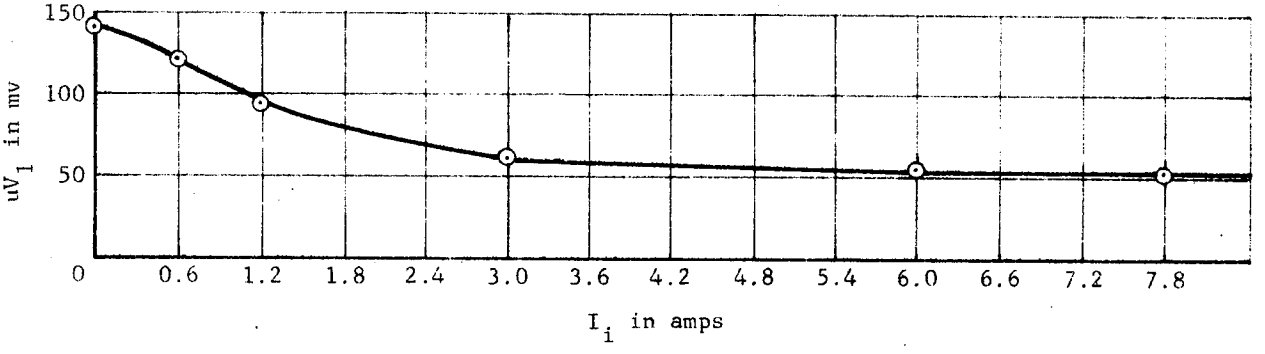


FIGURE D.3 uV_1 VS I_i I_W = MIN Q I_R = MAX Q

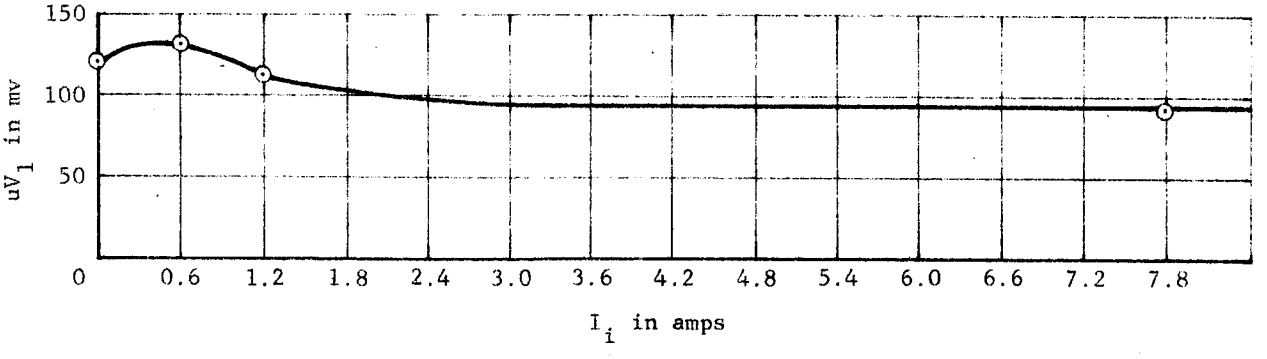


FIGURE D.4 uV_1 VS I_i I_W = MAX Q I_R = MIN Q

TABLE D.1 uV_1 MEASUREMENTS OF CONTROL SAMPLE "C"

Test Condition Temp -10° C	$I_R = I_W$ Min. Charge Program		I_R = Max Charge I_W = Min Charge		I_R = Min Charge I_W = Max Charge	
I_i (amps)	uV_1 (mv)	T_P (μsec)	uV_1 (mv)	T_P (μsec)	uV_1 (mv)	T_P (μsec)
0.000	119.0	0.98	139.0	0.72	122.0	1.12
0.600	101.0	0.90	122.0	0.68	133.0	1.12
1.200	075.0	0.80	90.5	0.64	116.0	1.08
1.800	066.0	0.80	79.1	0.63		
2.400	058.0	0.79	70.8	0.63		
3.000	056.0	0.79	67.4	0.62		
3.600	054.0	0.79	62.7	0.62		
4.200	052.2	0.79	61.6	0.62		
4.800	051.3	0.79	57.7	0.62		
5.400		0.79	57.0	0.62		
6.000	056.0	0.78	56.4	0.61		
6.600	053.6	0.78	54.2	0.61		
7.200	053.2	0.78	53.2	0.60		
7.800	052.7	0.78	52.2	0.60		
8.200	052.5	0.78	49.4	0.60	89.0	1.02

APPENDIX E

DETERMINATION OF uV_Z AS A FUNCTION OF WRITE/READ PROGRAM

Purpose

The purpose of this test is to determine the variations of uV_Z as a function of the write/read program and the inhibit pulse program. The test was conducted on Core C of the control sample at a temperature of -10° C.

Test Conditions

Test A uV_Z vs write/read program

The current program utilized in this test is shown in Figure E.1. Figures A.3 and A.4 of Appendix A are applicable for the test equipment setup and current driver schematics. The current program for this test is as follows:

I_R = minimum charge program

I_W = maximum charge program

$I_i = 0$

uV_Z is measured during step 2 read pulse time. The write pulse for various steps in the program is deenergized as noted and uV_Z and t_p recorded.

Test B uV_Z vs inhibit program

The current program utilized in this test is shown in Figure E.2. The charge program indicated for test A is applicable with I_i = 8 amp-turns. uV_Z is measured during step 2 read pulse time. The inhibit pulse is energized at the step write pulse time as indicated. uV_Z and t_p are recorded.

Test Results

The results of tests A and B are shown in Tables E.1 and E.2. uV_Z variations were severe showing a pronounced dependence upon the number of read pulses and the position of the inhibit pulse during the program. The variations noted in uV_Z were from 1.6 mv to 27.6 mv. Peaking time variations were from 0.48 μsec at 1.6 mv to 0.78 μsec at 27.6 mv.

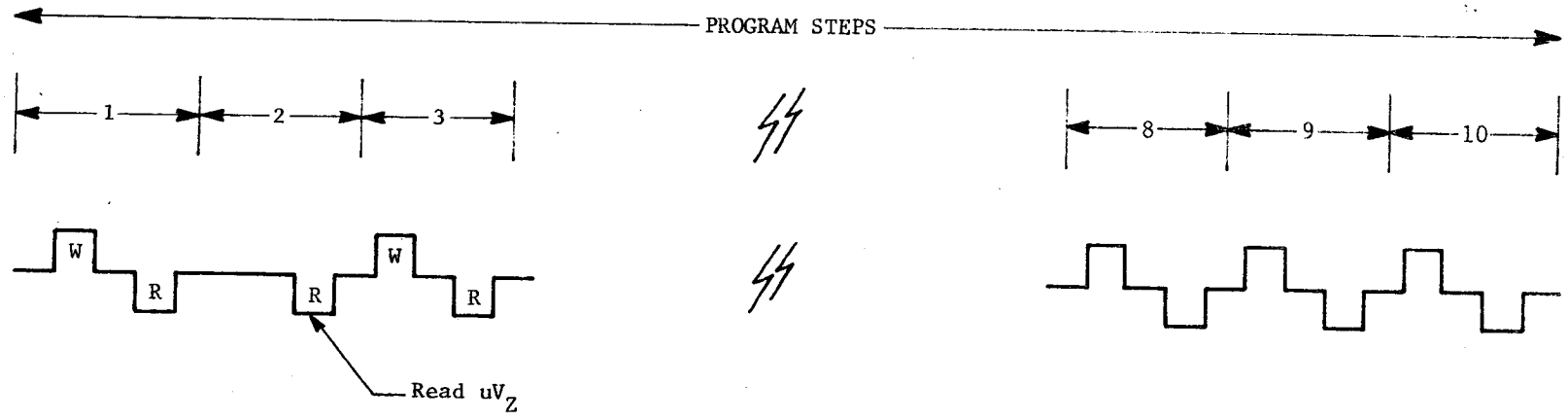


FIGURE E.1 CURRENT PROGRAM - TEST A

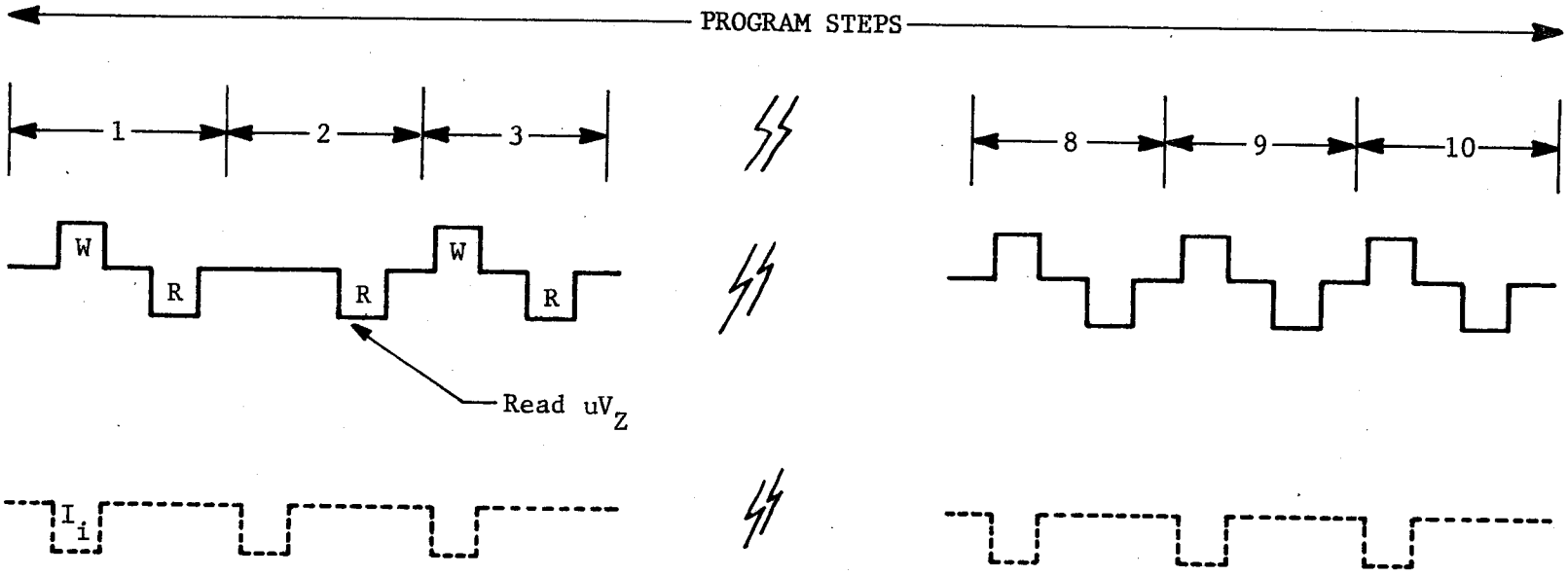


FIGURE E.2 CURRENT PROGRAM - TEST B

TABLE E.1 uV_Z MEASUREMENTS AT CYCLE TIME NO. 2

Test Conditions: I_W Deenergized Sequentially in a 10-Cycle Program

I_W Cycle Time Deenergized	uV_Z (mv)	t_p (μsec)
2	23.6	0.78
1	7.2	0.78
10	4.8	0.76
9	4.2	0.76
8	4.0	0.72
7	3.9	0.72
6	3.9	0.72
5	3.9	0.72
4	3.8	0.72
3	3.8	0.72

TABLE E.2 uV_Z MEASUREMENTS AT CYCLE TIME NO. 2

I_i Energized Cycle Time	uV_Z (mv)	t_p (μsec)
1	1.7	0.60
2	1.6	0.48
3	26.7	0.78
4	27.1	0.78
5	27.4	0.78
6	27.3	0.78
7	27.6	0.78
8	26.4	0.78
9	21.7	0.78
10	9.2	0.74

APPENDIX F

80-MIL COINCIDENT-CURRENT CORE SWITCHING CHARACTERISTICS

Purpose

The purpose of this test is to determine whether various types of 80-mil coincident-current cores displayed similar switching characteristics to that of core C of the control sample.

Test Conditions

Test A

Four units were tested at -10° C to the minimum charge program with and without the inhibit pulse uV_1 and t_p were recorded. The charge program is

$I_R = I_W$ = minimum charge pulse

I_i = 0 or 8 amp-turns.

Test samples included RCA 222M2, G.C. MC159, and two Ampex 802-40 units.

Test B

Two units were tested at -10° C to an unbalanced write/read program with and without the inhibit pulse. uV_1 and t_p were recorded. The current charge program was

I_R = maximum charge

I_W = minimum charge

I_i = 0 or 8 amp-turns.

Test C

Three units were tested to an unbalanced charge program with $I_i = 0$ at -10° C. uV_Z and uV_{Z2} were measured (see Appendix A). The current charge program was:

I_R = minimum charge

I_W = maximum charge

I_i = 0, uV_{Z1}, uV_{Z2}, t_{p1}, and t_{p2}

were recorded. Two units of the Ampex 802-40 and one unit of the G.C. MC159 core were tested.

Test Results

The results of tests A, B and C are tabulated in Table F.1. All of the devices tested exhibited similar switching characteristics to that of core C of the control sample. u_{V1} and uV_Z were extremely sensitive to the write/read and inhibit current programs.

TABLE F.1

Test Conditions	$I_R = I_W$ Minimum Charge Program				I_R = Minimum Charge I_W = Maximum Charge							
Inhibit I_i	$I_i = 0$		$I_i = 8.2$ amps		$I_i = 0$		$I_i = 8.2$ amps		Program A		Program B	
Core Type	uV_1 (mv)	T_p (μsec)	uV_1 (mv)	T_p (μsec)	uV_1 (mv)	T_p (μsec)	uV_1 (mv)	T_p (μsec)	uV_{Z1} (mv)	t_{p1} (μsec)	uV_{Z2} (mv)	t_{p2} (μsec)
RCA 222M2	170	0.98	96.80	0.87								
General Ceramics MC159	107	0.98	34.15	0.66	120	0.74	40.95	0.55	37.9	0.79	7.20	0.78
Ampex (JPL) 802-40	157	0.98	89.80	0.79					26.50	0.79	6.70	0.78
Ampex (Nort) 802-40	160	0.98	78.40	0.79	185	0.76	97.70	0.67	26.40	0.79	6.60	0.79

APPENDIX G

Proposed Process Specification No. 1

Title: Printed Circuit Board - JPL Inhibit Core Logic

1. SCOPE

1.1 Application - This specification established the requirements and acceptance criteria governing the printed circuit boards of the JPL Inhibit Core Logic. This specification constitutes the complete printed circuit board specification. In the event of conflict, the drawing requirements shall govern.

2. APPLICABLE DOCUMENTS

2.1 Application - The following are applicable to the extent specified herein.

Military Specifications and Standards:

MIL-P-13949	Plastic Sheet, Laminated, Copper Clad
MIL-G-45204	Gold Plating (Electrodeposited)
MIL-S-6872	Soldering Process, General Specification for
MIL-F-14256	Flux, Soldering, Liquid (Rosin Base)
MIL-P-55110	Printed Wiring Boards

Federal Specifications and Test Method Standard:

QQ-S-571	Solder, Tin-Lead Alloy
MIL-Std-202	Test Methods for Electronic and Electrical Parts
L-T-90	Tape, Pressure Sensitive, Adhesive
Fed. Test Method Std 151	Metals, Test Method

3. MATERIALS

Pressure Sensitive Tape	L-T-90 (Type I, Class A)
Isopropyl Alcohol, Technical	TT-I-735
Solder, Tin-Lead Composition Sn60 or Sn63	QQ-S-571

4. REQUIREMENTS

4.1 Workmanship - Printed circuit boards, including all parts and accessories, shall be fabricated, processed, and finished in a thoroughly workmanlike manner. Particular attention should be paid to plating, etching, soldering, cleaning and freedom from burrs and sharp edges.

4.2 Board Material - Vendor certification of board material, in accordance with applicable drawing call outs, shall accompany each vendor shipment. Board material shall meet the requirements of MIL-P-13949.

Title: Printed Circuit Board - JPL Inhibit Core Logic

4.3 Process Documentation - Process documentation consisting of (1) a description of each process, (2) the sequence of processes, and (3) process control parameters for each process, shall accompany each lot submitted by the vendor for qualification testing. Processes may not be changed without the written authorization of Materials and Process Engineering. Process certification is required as a condition of acceptance of all subsequent orders shipped by the vendor.

4.4 Photographic Pattern Processing - It is the responsibility of the vendor to determine that Engineering Master Patterns and Production Master Patterns are received in an undamaged condition and are capable of producing a printed circuit board within tolerance, before proceeding with subsequent processing.

4.4.1 Registration error shall not exceed 0.002 inch.

4.5 Plating - Pad surfaces shall be gold plated in accordance with MIL-G-45204, Type II, Class 2.

4.6 Etching - Immediately after completion of the etching process, the boards shall be processed to neutralize and remove etchant residues.

4.7 Identification - All markings shall be legible and free from defects such as smears and smudges. Markings, and/or overcoatings, are not permitted on pads or interconnection surfaces.

4.8 Soldering - All soldering shall be in accordance with MIL-S-6872, using Sn60 or Sn63 WARP Solder per QQ-S-571. Flux used shall be per MIL-F-14256, Type W.

4.9 Cleaning - Finished boards shall be thoroughly cleaned and dried before packaging for shipment. Boards shall be free of any contamination that will degrade solderability, insulation resistance, or cause corrosion products to form.

5. CIRCUITRY

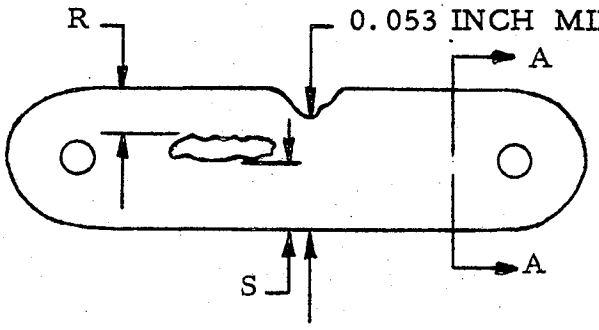
5.1 Pads

5.1.1 Spacing - Pad spacing shall be not less than 0.030 inch. Protrusions shall not reduce spacing to less than 0.030 inch. Protrusions longer than 0.020 inch are not acceptable.

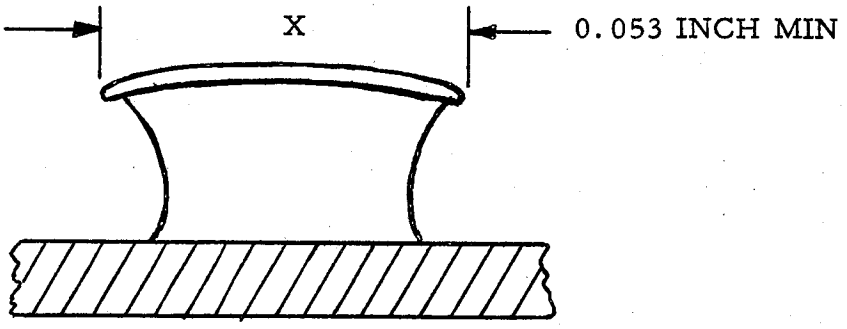
5.1.2 Isolated Metal Particles - Isolated metal particles shall not be permitted.

Title: Printed Circuit Board - JPL Inhibit Core Logic

5.1.3 Width - Pad width, as viewed from the surface of the board, shall be not less than 0.053 inch, excluding nicks and voids. See Figure 5.1.3.



R + S = 0.053 INCH MIN



SECTION A-A

Figure 5.1.3 - Pad Width

Title: Printed Circuit Board - JPL Inhibit Core Logic

5.1.4 Scratches and Pits - Scratches and pits shall not reduce pad cross section by more than 25 per cent. From the surface view, there shall be no exposed copper. See Figure 5.1.4.

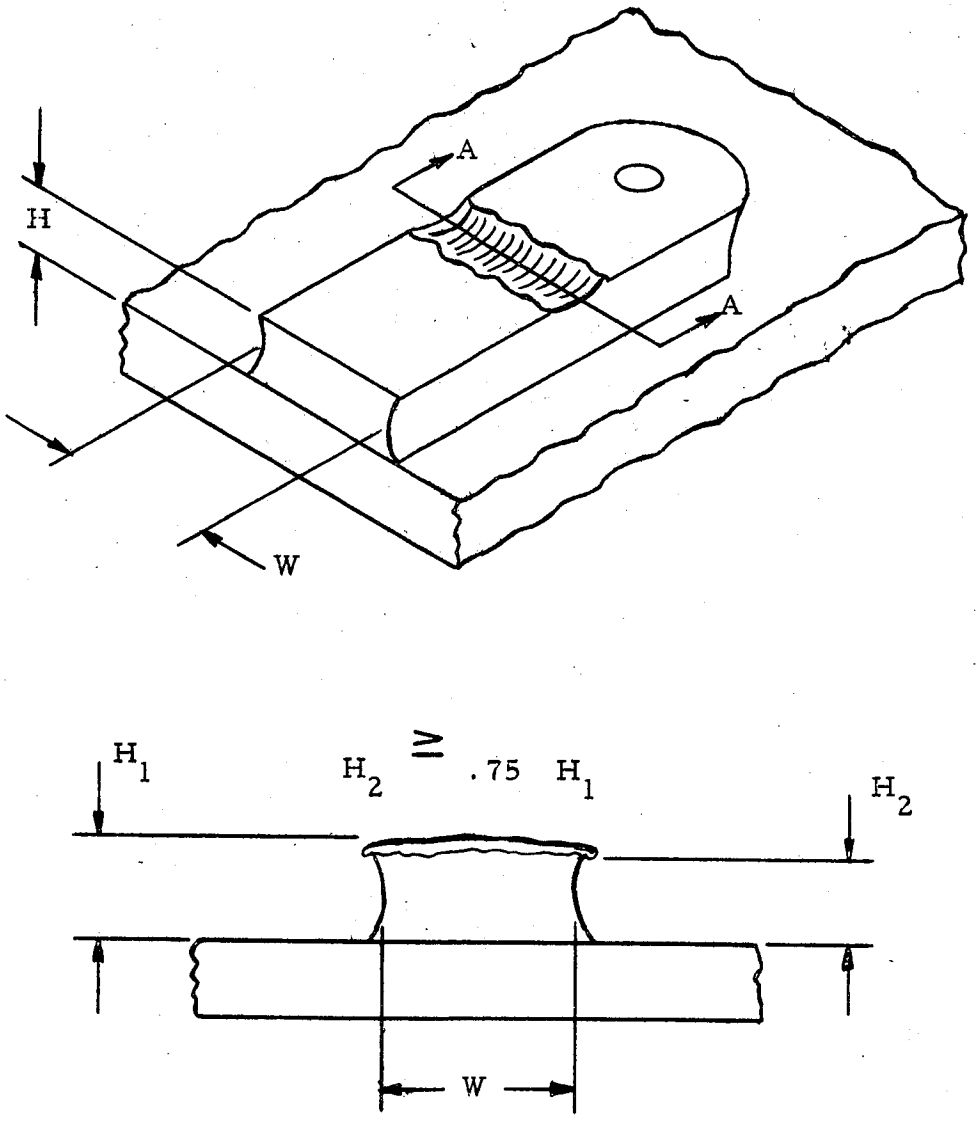
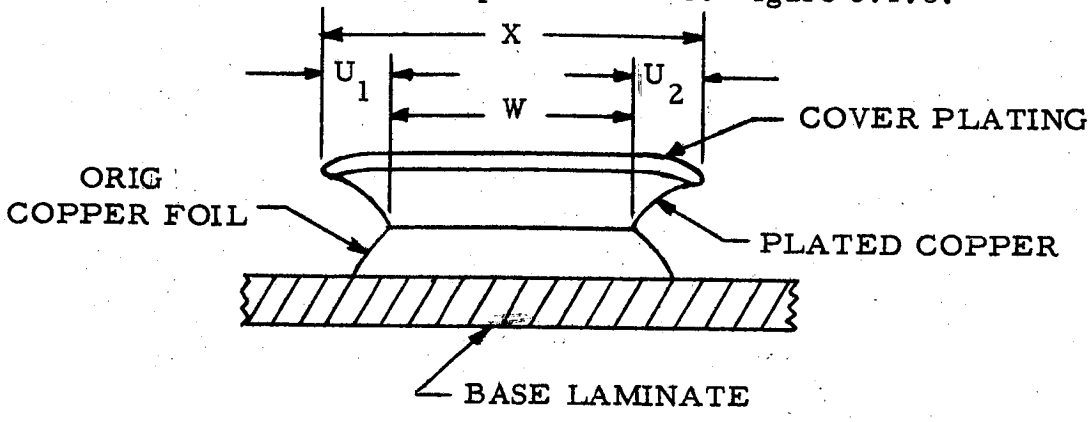


Figure 5.1.4 - Scratches and Pits

Title: Printed Circuit Board - JPL Inhibit Core Logic

5.1.5 Undercut and Overetch - Total undercut and overetch shall not exceed 0.003 inch per side. See Figure 5.1.5.

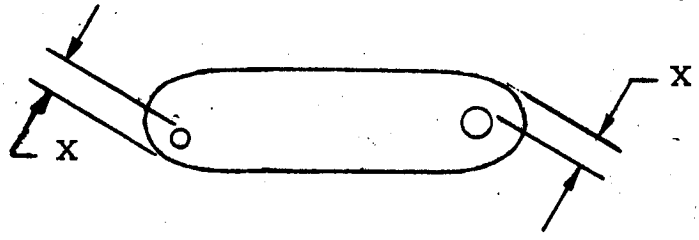


W = 0.047 INCH MIN
U_1, U_2 = 0.003 INCH MAX
X = 0.053 INCH MIN

Figure 5.1.5 - Undercut and Overetch

5.1.6 Circuitry Edge Distance - The circuit pattern of both front and back sides shall be centered on the board so that no part of the circuitry shall be closer than 0.005 inch to any edge of the finished board.

5.1.7 Hole - to - Pad Edge Distance - Hole edge to pad edge distance shall be not less than 0.010 inch. See Figure 5.1.7.



X = 0.010 INCH MIN

Figure 5.1.7 - Hole-to-Pad Edge Distance

5.1.8 Registration Error - Error shall not exceed 0.005 inch.

Title: Printed Circuit Board - JPL Inhibit Core Logic

6. FABRICATION

6.1 Warp - The maximum warp of the finished printed circuit board shall not exceed 0.010 inch per inch.

6.2 Twist - The maximum twist of the finished printed circuit board shall not exceed 0.010 inch per inch.

6.3 Delamination - Delamination of the base material shall not be permitted.

6.4 Edge Surface Finish - The edges of the base material shall have a surface finish of 63 Roughness Height Rating or better.

6.5 Mounting Holes - Mounting holes shall be located within 0.005 inch of the true position of the etched center lines on boards on which the mounting holes are located by crossed etched lines. See Figure 6.5.

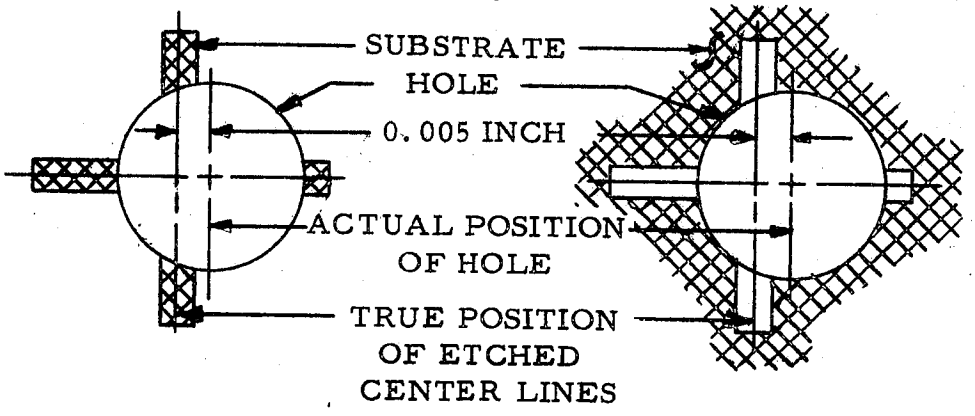


Figure 6.5 - Mounting Hole Location

7. QUALITY ASSURANCE

7.1 Qualification Testing - Qualification testing of all parts submitted for approval shall include all of the requirements of this specification.

7.1.1 Process Samples - Process samples shall be required as a condition of acceptance for each printed circuit board shipped by the vendor. The process samples shall be fabricated to the same configuration as those in the production lot and processed as part of the production lot. Sample quantities shall be determined by Quality Control.

7.2 Acceptance Inspection - Acceptance inspection of printed circuit boards shall consist of those examinations and tests deemed necessary to ensure compliance with this specification.

7.2.1 Sampling - Where a sampling plan of board characteristics or process samples is indicated, it is understood to be the minimum inspection level permissible. Nothing in the specification shall preclude the rejection of an entire lot should a lot sample fail to meet the requirements of this specification.

7.3 Material Review - Printed circuit boards submitted for acceptance that fail to meet the requirements of this specification shall be submitted to Material Review for disposition. Those boards determined not reworkable shall be conspicuously and permanently marked by drilling a hole (#30) in an area adjacent to the part number and returned to the vendor for scrap. Those boards considered reworkable may be reworked at the vendors' facility upon approval of the rework method by Materials and Process Engineering.

8. EXAMINATION AND TEST

8.1 Standard Test Conditions - Unless otherwise specified, all examinations and tests shall be conducted at room ambient temperature, atmospheric pressure, and a relative humidity of 55± 10 per cent.

8.2 Visual Examination - Surface features of printed circuit boards shall be normally examined using 7X magnification. Higher magnifications may be used to identify and analyze discrepancies.

8.3 Dielectric Withstanding Voltage - A test lot consisting of 12 test boards of the configuration described in Paragraph 4.5.2 and Figure 1 of MIL-P-55110 shall be tested for dielectric withstanding voltage per Paragraph 4.7.8 of MIL-P-55110. The test boards shall be fabricated from the same laminate material and processed under the same conditions used for production printed circuits boards. A conformal coating shall not be applied to the test sample boards for this test.

8.4 Temperature Cycling Test - There shall be no evidence of blistering, loss of bond strength, or separation of the metallic platings from themselves or from the substrate, when tested in accordance with the following procedure.

(a) Subject test specimen to temperature cycling in accordance with MIL-Std-202, Method 102A, Condition C except that low temperature shall be -80° F.

(b) Examine for compliance with the requirements of this test.

8.5 Plating Adhesion and Overhang Test - There shall be no evidence of separation between the plating and its substrates, nor shall there be any evidence of unsupported cover plating overhang removed or dislodged as a result of the following test.

(a) Apply a strip of pressure sensitive tape (Federal Specification L-T-90, Type 1, Class A) to the conductive area under test, using firm finger pressure. Apply parallel to conductor where possible.

(c) Examine the adhesive side of the tape and circuit edges under 7X magnification for compliance with this test.

(d) Remove adhesive residue from board by swabbing with isopropyl alcohol.

8.6 Plating Thickness Test - Plating thickness shall be determined by sectioning the test specimens and examining the plating thickness under a metallurgical microscope. Plating thickness shall be in accordance with Paragraph 4.6. The procedure shall be as follows:

(a) Section test specimen and prepare per Federal Test Method Std. 151, Method 521, for metallographic examination.

(b) Using a metallurgical microscope, read and record the plating thickness.

8.7 Conductor Cross Section and Under Cut Test - Conductor cross section shall be determined by sectioning the test specimens and examining under a microscope with a suitable reticle. See Figure 5.1.5.

8.8 Blister Test - There shall be no evidence of interlaminar blistering of the base material, or blistering and delamination of the copper foil. The procedure shall be as follows:

(a) Dip test specimen in suitable flux; drain excess flux.

(b) Float test specimen on solder pot containing Sn60 or Sn63 solder at 475 ±10° F for 20 seconds.

(c) Examine test specimen for compliance with this test.

Proposed Process Specification No. 1

Title: Printed Circuit - JPL Inhibit Core Logic

9. CLASSIFICATION OF DEFECTS AND RECEIVING INSPECTION CRITERIA

Description	Spec. Reference Para.	Test Procedure Para.	Classification of Defects
Workmanship	4.1		Major
Board Material	4.2		Major
Production Processes	4.3		Major
Plating Type	4.5		Major
Identification	4.7		Major
Pads:			
Plating Thickness	4.5	8.6	Major
Spacing	5.1.1		Critical
Isolated Metal Particles	5.1.2		Critical
Width	5.1.3		Major
Scratches and Pits	5.1.4		Major
Undercut/Overetch	5.1.5	8.7	Major
Circuitry Edge Distance	5.1.6		Major
Hole to Edge Distance	5.1.7		Major
Circuit Registration	5.1.8		Major
Fabrication:			
Warp	6.1		Major
Twist	6.2		Major
Delamination	6.3		Major
Edge Surface Finish	6.4		Major
Mounting Holes	6.5		Major
Tests:			
Dielectric Withstanding Voltage	8.3	8.3	Critical
Temperature Cycling	8.4	8.4	Critical
Plating Adhesion and Overhang	8.5	8.5	Critical
Plating Thickness	4.6	8.6	Major
Conductor Cross Section and Undercut	5.1.5	8.7	Major
Blister	8.8	8.8	Critical

Proposed Process Specification No. 2

Title: EMBEDMENT OF CORE LOGIC BOARD

1. INTRODUCTION

This document covers the materials and procedures for embedding ferrite core laminated boards.

2. PROCEDURE

2.1 Cleaning - Clean the core logic boards in a vapor degreaser with trichloroethylene solvent for several minutes or by immersing the boards in a tray of trichloroethylene solvent for 1 to 2 minutes. Dry the boards on paper towels for 5 ±1 minute, then insert the boards in an oven at 150° ±5° F for 10 to 15 minutes to remove all traces of the solvent.

2.2 Bonding of Epoxy Laminate Mold -

2.2.1 EC-1614 Adhesive Preparation - Weigh out 1 part by weight of Part A to 1 part by weight of Part B in a clean container and mix the 2 components together thoroughly with a wooden spatula until a homogeneous mixture is obtained.

2.2.2 Application of EC-1614 Adhesive - Apply a thin layer, 5 to 10 mils, of the mixed adhesive on the bonding edge of the mold with a wooden spatula.

2.2.3 Joining - Carefully index the permanent laminate mold in the proper area, above the core logic board. Bring the two surfaces together, taking care that the relative positions of the parts are not changed. Slowly join the two parts from the initial contact edge to the opposite edge. Place a uniform compressive load of approximately one pound on the joined parts so that an intimate contact is maintained. Apply a small fillet of the mixed adhesive around the outer periphery of the glue-line to render the joined surfaces leak-proof.

2.2.4 Curing - Cure the bonded assembly in an oven at 150° ±5° F for 1 hour ±5 minutes. Remove the compressive load after cure.

2.3 Primary Embedment with RTV-11

2.3.1 Priming - Apply a thin coating of D.C. 4094 primer on all surfaces where RTV-11 sealant will come in contact. Allow primer to air-dry for at least 30 minutes prior to sealant application.

Title: EMBEDMENT OF CORE LOGIC BOARD

2.3.2 Preparation of RTV-11 Silicone Sealant - Weigh out 0.1 parts by weight, Thermolite 12 catalyst to 100 parts by weight RTV-11 silicone sealant in a clean container. Mix the 2 components together thoroughly with a spatula until a homogeneous mixture is obtained. Vacuum degass the mixture at 5 ±1 mm mercury pressure for 5 ±1 minutes. Use the mixed sealant within 35 ±5 minutes after the addition of the catalyst.

2.3.3 Embedding - Slowly pour the mixed sealant into the mold cavity so that air entrapment is avoided. Add sealant into the cavity until the level of the sealant is between 1/32 inch to 1/16 inch above the top of the ferrite cores. Keep the assembly level at all times.

2.3.4 Curing - Cure the silicone sealant at 150° ±5° F oven temperature for 5 hours ±10 minutes.

2.4 Secondary Embedment with Scotchcast No. 241

2.4.1 Preparation of Scotchcast No. 241 Epoxy Casting Resin - Weigh out 1 part by weight Part A to 2 parts by weight Part B. Mix the 2 components together thoroughly with a spatula. Heat the mixture to 160° ±5° F and vacuum degass the mixture at 5 ±2 mm of mercury pressure for 3 ±1 minutes.

2.4.2 Embedding - Slowly pour the warmed mixed resin on top of the cured RTV-11 sealant in the mold cavity until the casting resin is level with the top edge of the permanent mold. Keep assembly level at all times.

2.4.3 Curing - Cure the cast resin at 180° ±5° F oven temperature for at least 5 hours.

3. INSPECTION REQUIREMENTS

3.1 Critical

3.1.1 There shall be no visible evidence of surface air bubbles or voids on the embedding materials.

3.1.2 The respective cure cycles for EC-1614, RTV-11, and Scotchcast No. 241 shall be strictly followed.

3.2 Major

3.2.1 The permanent mold shall be properly aligned on the core logic boards after bonding.

3.2.2 There shall be no visible sign of contamination on the core logic board assembly prior to embedding.

Title: EMBEDMENT OF CORE LOGIC BOARD

4. MATERIALS REQUIREMENTS

The physical and electrical properties of the embedment materials shall be as listed below.

4.1 RTV-11, Silicone Sealant with 0.1% Thermolite 12 Catalyst

Specific Gravity	1.18
Durometer, Shore A	45
Tensile Strength, psi	350
Elongation, %	180
Tear Strength, lbs/in, Die B	15
Peel Strength, lbs/in (bonded to 304 stainless steel, SS-4004 primed)	3
Linear Shrinkage, %	0.5
Dielectric Strength (70 mils thickness)	450 V/mil
Insulation Resistance, ohm-cm	6.0×10^{14}
Dielectric Constant	
60 cycles (RT)	3.6
1 Mc (RT)	3.4
Power Factor, %	
60 cycles	1.9
1 Mc	0.50

4.2 Scotchcast No. 241, Epoxy Casting Resin

Specific Gravity	1.42
Hardness, Shore D	60
Linear Shrinkage, %	0.8
Mechanical Shock Resistance (MIL-I-16923C)	no cracking
Thermal Shock Resistance (10 cycles -55°C to 130°C 3M 1/4 inch insert)	no cracking
Heat Resistance (% wt loss at 130°C MIL-I-16923C)	0.57
Moisture Absorption (% wt increase 240 hours at 96% RH MIL-I-16923C)	0.6

Title: EMBEDMENT OF CORE LOGIC BOARD

Thermal Conductivity (Cal/sec/cm^2/°C/cm, MIL-I-16923C)	8.0×10^{-4}
Dielectric Strength, V/mil	375
Dielectric Constant	
100 cycles (RT)	5.5
1 Mc (RT)	3.6
Dissipation Factor	
100 cycles (RT)	.08
1 Mc (RT)	.03
Volume Resistivity, ohm/cm	1×10^{14}

5. APPLICABLE DOCUMENTS

Military Specification

MIL-I-16923 Insulating Compound, Electrical, Embedding

6. MATERIALS AND SPECIAL EQUIPMENT

Trichloroethylene, Solvent	Commercially available
Cheesecloth	Commercially available
Oven, Stabil-Therm or equivalent	Blue M Electric Co.
EC-1614, Epoxy-Polyamide Adhesive	Minnesota Mining & Manufacturing, Los Angeles, Calif.
Mold, Epoxy Laminate, MIL-P-18177, Type GEE	Commercially available
RTV-11, Silicone Sealant	General Electric Co.
Vacuum Equipment, Cenco Hypervac 23 or equivalent	Central Scientific Co., Chicago, Illinois
DC 4094, Primer	Dow Corning Corp., Midland, Michigan
Scotchcast No. 241 Epoxy Casting Resin	Minnesota Mining & Manufacturing, Los Angeles, Calif.

Proposed Process Specification No. 3

Title: WIRING OF JPL INHIBIT CORE LOGIC MODULE

1. SCOPE

This specification covers the procedure for wiring a JPL inhibit core logic module.

CAUTION

Handle ferrite cores carefully. They are extremely brittle and will chip easily. Discard any core which has been dropped on any surface other than the foam pad provided for the work bench. Use plastic tipped tweezers for handling cores.

Allow cores to move of their own weight when strung on wires. If cores must be moved by hand, push them into place with plastic tipped tweezers.

2. PROCEDURE

2.1 Place a quantity of cores in the core shaker plate.

2.2 Place core shaker plate on mechanical shaker and vibrate for two minutes. If mechanical shaker is not available, the core shaker plate can be vibrated by hand.

2.3 Inspect core shaker plate for assurance that all cores are in the slots. Any core not in the slot can be placed in position with plastic tipped tweezers.

2.4 Apply mastic tape 2 inches over the core shaker plate and press the tape with hand or roller over cores.

2.5 Remove the tape from the core shaker plate and place on the assembly jig.

2.6 String No. 30 AWG insulated copper wire through each row of cores in the X axis.

2.7 String No. 30 AWG insulated copper wire through each row of cores in the Y axis.

CAUTION

When using No. 30 AWG, all cores are at 45° angles to vertical axis of the assembly jig. The cores can be broken loose from the mastic tape.

2.8 Inspect cores for proper angle of 45°.

2.9 Remove this assembly from the assembly jig by the X and Y wires.

Title: WIRING OF JPL INHIBIT CORE LOGIC MODULE

2.10 Place this assembly on the printed circuit board and terminate each wire, per proposed Process Document No. 4.

2.11 Remove from "prepared wire strip" the wire which corresponds to the first winding diagram.

2.12 Insert and bend stripped and tinned wire end into inboard hole of input termination pad indicated on wiring diagram.

2.13 Following wiring diagram thread wire around pegs indicated, through and around cores indicated, finishing at output termination pad indicated on wiring diagram. Use plastic tipped tweezers or hooks to pull or push the wire through the routing sequence.

2.14 Insert and bend pre-stripped and tinned end of wire into inboard hole in termination pad.

2.15 Place electrical test fixture in position and check for proper winding sequence.

2.16 Solder both ends of wire on core side of board using 50-50 (Sn 50) solder at normal wiring temperature.

2.17 Turn wiring diagram card to new card and repeat 2.11 through 2.16.

Proposed Process Specification No. 4

Title: PREPARATION AND TERMINATION OF MAGNET WIRE

1. SCOPE

1.1 Application - This specification establishes requirements governing cutting, stripping, and termination of magnet wires used on the inhibited logic memory assembly. The requirements are applicable when this specification is called out on a drawing or related document. In the event of conflict, the drawing requirements shall govern.

2. APPLICABLE DOCUMENTS

2.1 Application - The following are applicable to the extent specified herein.

Military Specification

MIL-W-583	Wire, Magnet, Electrical

Federal Specification

QQ-S-571	Solder, Soft (Tin, Lead, Tin-Lead)

3. MATERIALS

3.1 The following are applicable to the extent specified herein.

Wire Stripper, Lonco #3111HH	Claude Michael Inc. Glendale, Calif.
Sodium Bicarbonate	Commercial
Ultrasonic Cleaner	Delta Sonics Hawthorne, Calif.

4. REQUIREMENTS

4.1 Wire Stripping

4.1.1 Wire Cutting - Wires shall be cut and stripped to length per drawing callout.

4.1.2 Insulation Removal - Wire insulation shall be removed by immersing the wire section that is to be stripped in Lonco 3111HH wire stripper at room temperature for 60-90 seconds "wiping" the insulation off between absorbent tissue. Absorbent tissue shall only be used once.

4.1.3 Post Stripping Process - The stripped section of the wire shall be immediately immersed in an ultrasonically agitated solution of 10 percent sodium bicarbonate for 2-5 seconds followed by two water rinses. Wire shall be carefully dried by wiping between absorbent tissue.

Title: PREPARATION AND TERMINATION OF MAGNET WIRE

4.1.4 Stripping Inspection Criteria - Insulation shall be completely removed without damaging the conductor.

4.1.5 Time Limit Prior to Soldering - Termination shall be done within forty-eight hours after stripping.

4.2 Wire Termination

4.2.1 Soldering - Wires shall be soldered per proposed Process Document No. 6.

4.2.2 Wire Termination Inspection - Wire termination shall be inspected to assure that solder joints meet inspection criteria of proposed Process Document No. 6 on both sides of the board and that cut end of the wire is visible.

Proposed Process Specification No. 5

Title: CIRCUIT BOARD IDENTIFICATION

1. INTRODUCTION

This specification covers the application of markings, such as assembly numbers, part numbers, and serial numbers, directly to the surface of printed circuit boards.

2. PROCEDURE

2.1 General Requirements

2.1.1 Precautions - Printed circuit boards are delicate, expensive parts. Take extreme care to avoid any damage to the board or to its components during application of markings.

2.1.2 Application Methods - Apply markings by silk screen or with a pen or fine brush. Selection of a particular method is dependent on type of marking (fixed or variable), number of circuit boards, stage of assembly, etc.

2.1.3 Location - Apply markings in locations specified on drawings. Do not apply markings on any conductors or solder pads. If location is not specified, apply the marking on the back side of the board in a suitable area.

2.1.4 Size - Use the size of marking specified on the drawing. If size is not specified, use a height of marking from 1/16 inch minimum to 1/8 inch maximum, depending on area available.

2.2 Silk Screen Application

2.2.1 Mixing of Material - Prepare a sufficient quantity of material to last till the end of the shift (3 ounces maximum) by thoroughly mixing 6 parts of Catalyst 20 with 100 parts of Cat-L-Ink (white) by weight on a piece of acrylic sheet. Pot life will be approximately 8 hours.

2.2.2 Application

2.2.2.1 Holding the printed circuit board by the edges, place the board in its nest in the acrylic holding fixture with bottom (non-component) side up. The acrylic holding fixture ensures off-contact printing.

2.2.2.2 Clamp the silk screen frame into the carriage and swivel mount.

2.2.2.3 Position silk screen mask over the printed circuit board, carefully registering the part number pattern over the proper area on the board.

2.2.2.4 Lock the swivel mount into position.

2.2.2.5 Squeegee a layer of Cat-L-Ink over the entire surface of the silk screen pattern. Remove the silk screen.

2.2.2.6 Holding the printed circuit board by the edges, position the board in the tree-type holding rack.

2.2.2.7 Allow the markings to air-dry 3 hours before handling and overnight before packaging, or force dry for 1 hour at 150° F before handling or packaging.

2.2.2.8 Place each identified board in its individual envelope in accordance with requirements of the Materials Handling Manual.

2.3 Pen or Brush Application

2.3.1 Mixing of Material

2.3.1.1 Use Wornowink No. 9 White, M-9-N for marking.

2.3.1.2

Material	Proportions
Wornowink No. 9 White	100 parts by weight
Wornowink Air-Cure Catalyst, Solution A	5 parts by weight
Wornowink Thinner T-1	15 cc per 100 parts of #9

Mix the above proportions thoroughly in a glass container. Pot life will be approximately 8 hours at 75° F. Additional T-1 thinner may be added, as necessary, if material becomes too thick toward the end of its pot life.

2.3.1.3 Wornowink No. 9 may be obtained in a 1-ounce kit. If 1-ounce kits are used, mix the entire contents of the vial of Air-Cure Catalyst A with the 1-ounce can of Wornowink No. 9 white. Add approximately 4 cc of T-1 thinner and mix thoroughly.

2.3.2 Application

2.3.2.1 Apply marking using an ordinary pen dipped lightly into the mixed ink or by means of a fine-tipped, camel's hair, artist's brush.

2.3.2.2 Apply the markings in a clear, legible manner. Remove smeared markings by wiping lightly with a clean cloth wet with MX-4 solvent.

2.3.2.3 Position the marked board in the tree-type holding rack. Air-dry the markings 3 hours before handling and overnight before packaging, or force-dry for 1 hour at 150° F before handling or packaging.

2.3.2.4 Place each identified board in its individual envelope in accordance with requirements of the Materials Handling Manual.

3. INSPECTION REQUIREMENTS

3.1 Critical

3.1.1 When thoroughly cured, the marking shall have a hard finish, free of blisters, and shall be clearly legible.

3.1.2 The cured marking shall not be removable using MX-4 solvent.

3.1.3 Markings shall not be over any conductors or solder pads.

4. MATERIALS AND SPECIAL EQUIPMENT

Wornow Cat-L-Ink No. 50-100 (White)	Wornow Process Paint Co., Los Angeles, Calif.
Wornow Cat-L-Ink No. 20 Catalyst	Wornow Process Paint Co.
Wornowink No. 9 White, M-9-N, and Wornowink Air-Cure Catalyst A (1-ounce kit)	Wornow Process Paint Co.
Wornowink T-1 Thinner	Wornow Process Paint Co.
MX-4 Solvent	John B. Moore Co., Los Angeles, Calif.
Acrylic Holding Fixture	Nortronics Tool
Board Tree Rack	Nortronics Tool

Proposed Process Specification No. 6

Title: PRINTED CIRCUIT BOARD ASSEMBLY - SOLDERING

1. INTRODUCTION

This specification covers soldering when required on printed circuit board assemblies.

2. PROCEDURE

2.1 General

2.1.1 Turn soldering iron on and allow it to warm up for 3 minutes minimum to reach operating temperature.

2.1.2 Mix flux and thinner in a 1 to 4 ratio by volume in a flux container.

2.1.3 Pour MX-4 solvent into solvent container.

2.1.4 Install circuit board in holding fixture.

2.1.5 Adjust magnifying lamp over holding fixture as required.

2.1.6 Clean tip of soldering iron as required.

→ 2.1.7 Discard solvent every 4 hours or oftener at the discretion of Manufacturing.

2.2 Touchup

→ 2.2.1 Apply flux mixture with brush to side of joint requiring touchup.

2.2.2 Apply heat to the back (non-component) side of the circuit board only long enough to obtain proper wetting and solder flow (2-5 seconds, depending on the size of the joint). Where additional solder is needed, add only enough to obtain proper fillet formation.

2.2.3 Use tip of soldering iron to carefully reflow and remove any icicles or bridges.

2.2.4 Remove flux residue from localized areas with brush dipped in solvent.

→ 2.2.5 Air-dry for 5 minutes minimum. A filtered air blast may be used, provided that air pressure does not exceed 35 psi.

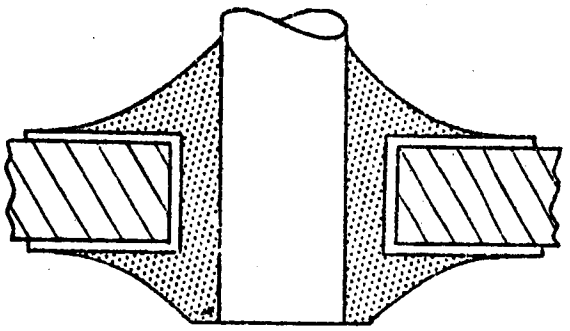
→ Indicates Change

Title: PRINTED CIRCUIT BOARD ASSEMBLY - SOLDERING

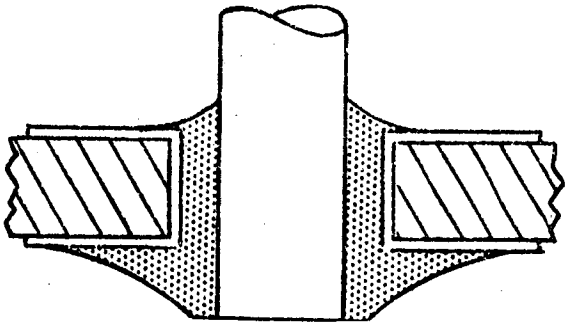
3. INSPECTION REQUIREMENTS

→ 3.1 Critical

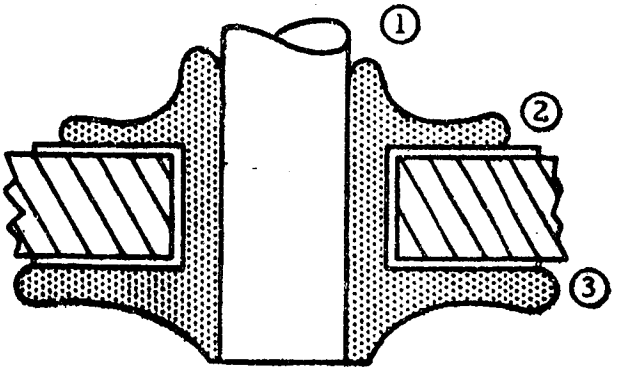
3.1.1 Solder Flow and Adhesion



Solder joint, as shown, is IDEAL. Solder flow is adequate, and adhesion to lead and pad on both sides of the board is intimate, showing a slightly concave fillet which extends out to a feather edge on both sides of the pad and the front side of the conductor lead.

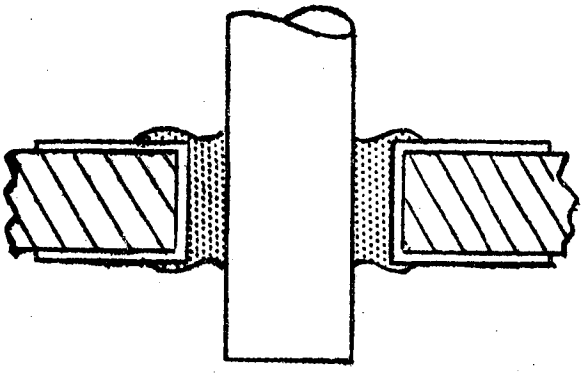


ACCEPTABLE. Solder adhesion to lead on component side of board is indicated by the minute fillet radius.



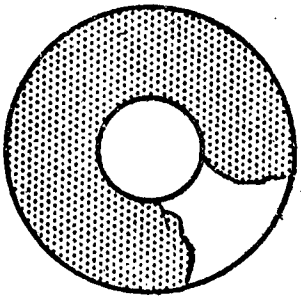
NOT ACCEPTABLE. Lack of adhesion indicated by evidence that (1) wire is not wet on component side, or (2) that pad is not wet at the solder-pad interface. (3) Excess solder is indicated by the extension of solder past the edge of the pad.

Title: PRINTED CIRCUIT BOARD ASSEMBLY - SOLDERING

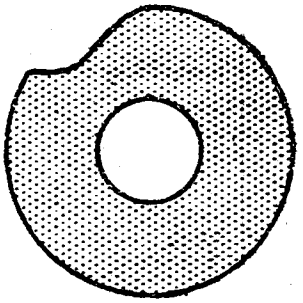


NOT ACCEPTABLE. Insufficient solder indicated by lack of fillet on either or both sides of board.

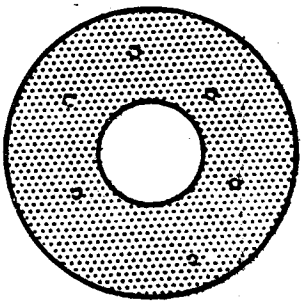
3.1.2 Solder Voids and Pinholes



ACCEPTABLE. Solder voids which are less than 25 percent of pad area are acceptable providing void does not extend beneath board surface.

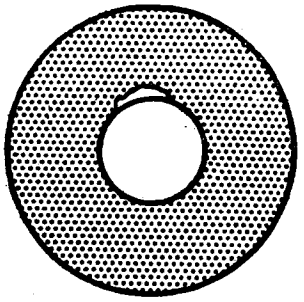


ACCEPTABLE. Any minor cutouts on pad are acceptable providing solder joint is not affected. Make void shown slightly smaller around circumference (same width).



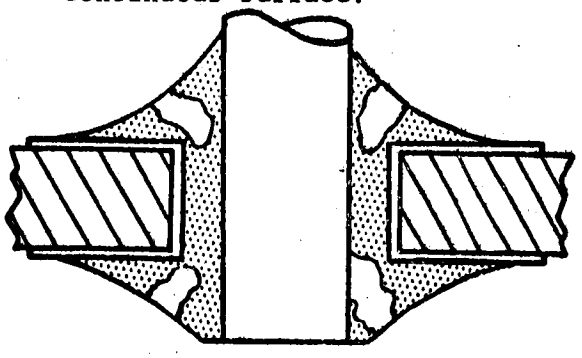
ACCEPTABLE. Pinholes not directly adjacent to component lead.

Title: PRINTED CIRCUIT BOARD ASSEMBLY - SOLDERING

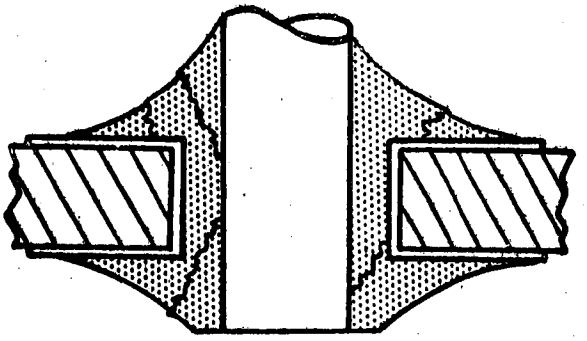


ACCEPTABLE. Lack of adhesion between solder and component lead is acceptable providing it does not exceed 25 percent of the component lead circumference.

3.1.3 Solder Appearance - Solder joints shall present a smooth, continuous surface.



NOT ACCEPTABLE. Holes in joint indicate major voids or rosin entrapment.



NOT ACCEPTABLE. Fracture lines on surface of joint indicate a cold or disturbed joint.

3.1.4 Bridges - No solder bridges are permitted. Solder flow must follow the contour of the etched circuitry.

3.1.5 Icicles - No icicles are permitted.

3.2 Major

→ 3.2.1 Assemblies shall be visibly free of flux residue after cleaning.

3.2.2 The specific gravity of the flux - flux thinner mixture shall be maintained between 0.82 and 0.84 at ambient temperature by the addition of the flux thinner.

→ 3.2.3 Solvent shall be discarded every 4 hours or oftener at the discretion of Manufacturing.

Title: PRINTED CIRCUIT BOARD ASSEMBLY - SOLDERING

4. MATERIALS AND SPECIAL EQUIPMENT

Resin Flux, Kester No. 1544	Claude Michael Agency, Glendale, California
Flux Thinner, Kester Formula 104	Claude Michael Agency
Solvent, Moore Chemical Company MX4	Arthur K. Meyer Company Los Angeles, California
Solder, Sn60Pb40, Kester 44 Resin Core, 0.035 inch maximum diameter, or equivalent	Claude Michael Agency
Soldering Iron, Oryx 6 Watt Model 6A	Claude Michael Agency

APPENDIX H

TEST PROCEDURES

1. SCRAPE-RESISTANCE TEST

1.1 Purpose - The purpose of this test is to compare various types of magnet wire insulation for resistance to the scraping effects of ferrite cores as the wires are passed through the cores.

1.2 Setup - The setup for this test is shown in Figure H.1. The 90-volt supply provides a current of 10 ma when the film coating has been sufficiently abraded to cause dielectric failure. This abrasion is detected by the bare copper No. 20 AWG wire as the test wire passes under.

1.3 Procedure

1.3.1 Set up meter, battery, sensing wire and core as shown in Figure H.1.

1.3.2 Strip one end of the test wire and thread it through the core as shown in Figure H.2. Connect this wire to the test circuit.

1.3.3 Attach a five-gram weight to the unstripped end of the wire.

1.3.4 Pull the wire through the core at a rate of approximately 60 cycles per minute at an excursion in each direction of 1/2 inch.

1.3.5 Record the number of cycles required to get a failure indication as the test wire passes under the sensing wire.

1.3.6 Replace the ferrite core between tests to insure uniform abrading surfaces for all tests.

1.4 Materials

1) No. 38 AWG copper test wire
2) Insulation materials: Heavy Formvar, Heavy Polythermaleze, and Heavy ML
3) Ampex electric 802-40 ferrite cores.

2. ABRASION RESISTANCE TEST

2.1 Purpose - The purpose of this test is to compare various magnet wire insulation materials for resistance to abrasion as the wires pass over the surface of ferrite cores.

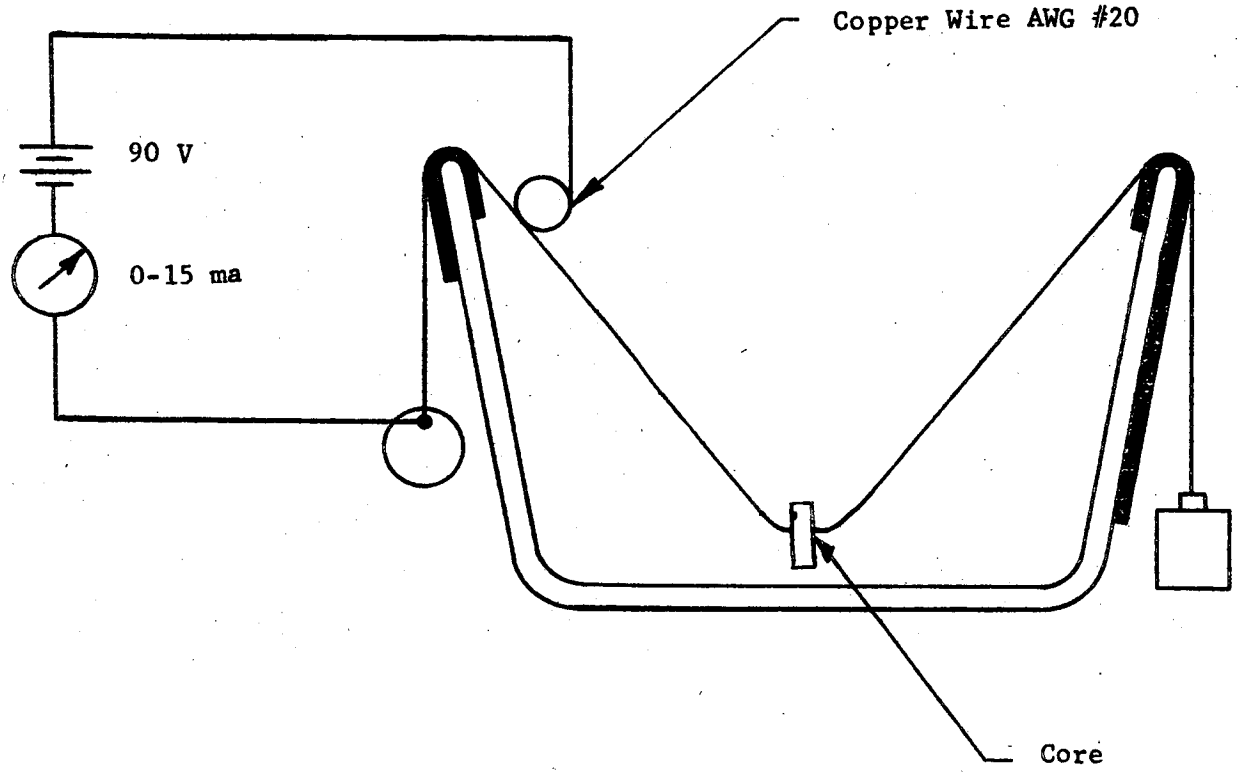


FIGURE H.1 TEST SET-UP SCRAPE RESISTANCE TEST

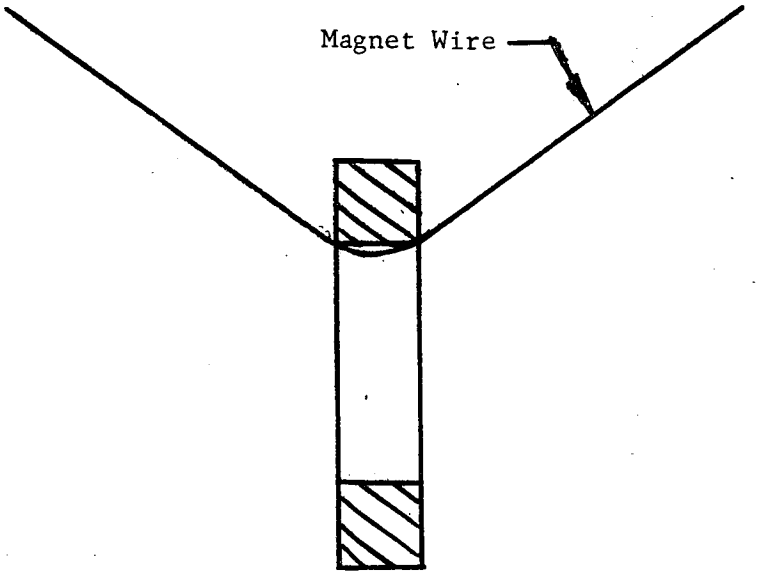


FIGURE H.2 THREADING OF WIRE THROUGH CORE

2.2 Setup - The setup for this test is shown in Figure H.3. Insulation failure is indicated by a 10 ma deflection of the meter with a current path through the electrolyte.

2.3 Procedure

2.3.1 Remove insulation from one end of the test wire. Set up as shown in Figure H.3. Attach 5-gram weight.

2.3.2 Pull the wire past the core at a rate of about 60 cycles per minute with a total excursion in each direction of 1/2 inch.

2.3.3 Record the number of cycles to failure.

2.3.4 Repeat with new abrading surface using a 20-gram weight.

2.4 Materials

1) No. 38 AWG copper test wire
2) Insulation materials: Heavy Formvar, Polythermaleze, and Heavy ML
3) Sodium Chloride electrolyte
4) Ampex electric 802-40 and 480-67, Electronic Memories No. 81-104 and 81-101A and Lockheed 80-04 ferrite cores.

3. CUT-THROUGH RESISTANCE TEST

3.1 Purpose - The purpose of this test is to compare the cut-through resistance of various insulation materials used on magnet wire and to determine improvement, if any, when the cores are coated to reduce surface irregularities.

3.2 Setup - The setup for this test is shown in Figure H.4. Failure of the insulation due to cutting is indicated by a 10-ma deflection on the meter.

3.3 Procedure

3.3.1 Strip insulation from one end of the test wire.

3.3.2 Wrap test wire two turns through the ferrite core. Tighten each turn by suspending a 100 gram weight from the unstripped end of the test wire while holding the stripped end fixed.

3.3.3 Completely submerge the ferrite core-test wire assembly in the electrolyte. The wire ends must remain out of the electrolyte throughout the test. Agitate the core and wire until all air bubbles are dissipated from the core-wire interface areas.

3.3.4 Connect the circuit.

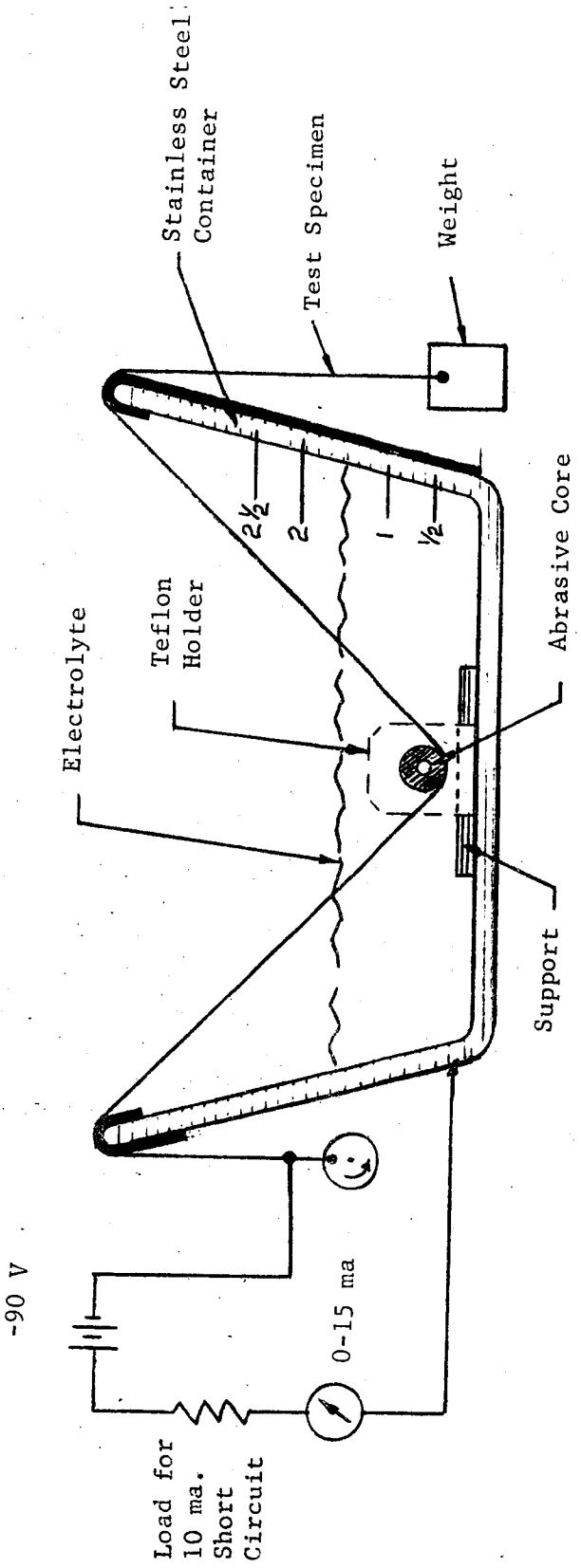


FIGURE H.3 SET-UP FOR ABRASION RESISTANCE TEST

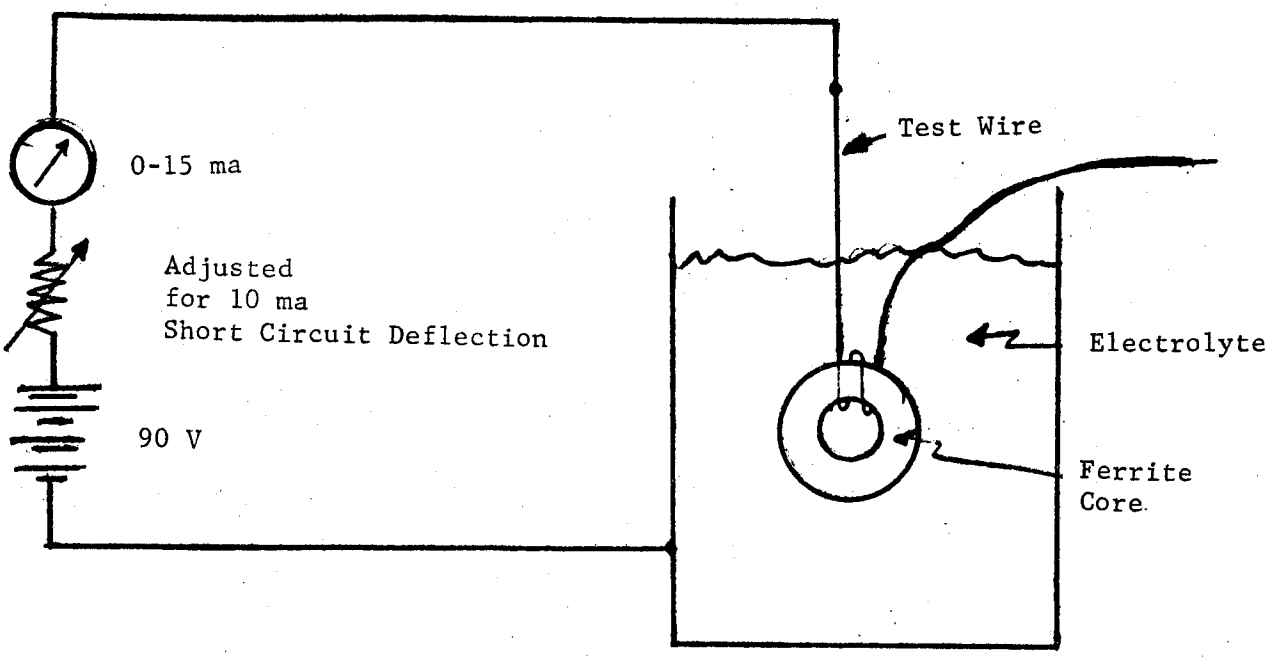


FIGURE H.4 SET-UP FOR CUT-THROUGH RESISTANCE TEST

3.3.5 Record success or failure of test wires.

3.3.6 Test each insulation type with uncoated and coated cores.

3.4 Materials

1) No. 38 AWG copper magnet wire
2) Insulation: Heavy Formvar, Heavy Solvar and other insulation coatings as deemed desirable
3) Lockheed Electronics 80-04 ferrite cores
4) 5 percent solution of sodium chloride electrolyte
5) Krylon coating for ferrite cores.

4. EMBEDMENT STRESS TEST

4.1 Purpose - The purpose of this test is to define the effects of embedment stresses on the electrical characteristics of ferrite cores.

4.2 Test Specimens - The configuration of the test specimens is shown in Figure H.5. Two No. 38 AWG insulated copper wires are inserted into a core at right angles as they pass through the core. These are soldered to the test terminals. Additionally, 20 unterminated No. 38 AWG wires are inserted into the core to simulate worst-case conditions.

4.3 Procedure

4.3.1 Upon completion of the test specimens, have sensing wires checked for electrical continuity and the ferrite core for its magnetic parameters.

4.3.2 Embed the test specimen (masking the terminals) in accordance with proper mixing, pouring and curing instructions for the embedment material.

4.3.3 Upon completion of the cure cycle, have the core magnetic characteristics re-measured.

4.3.4 Compare before and after characteristics.

4.4 Materials

1) No. 38 AWG insulated copper wire
2) Ampex 81-104 ferrite cores
3) Terminal Boards
4) Embedment Systems:
   a) Epoxy
   b) RTV-11 with epoxy overcoat
   c) Sylgard 182 with epoxy overcoat.

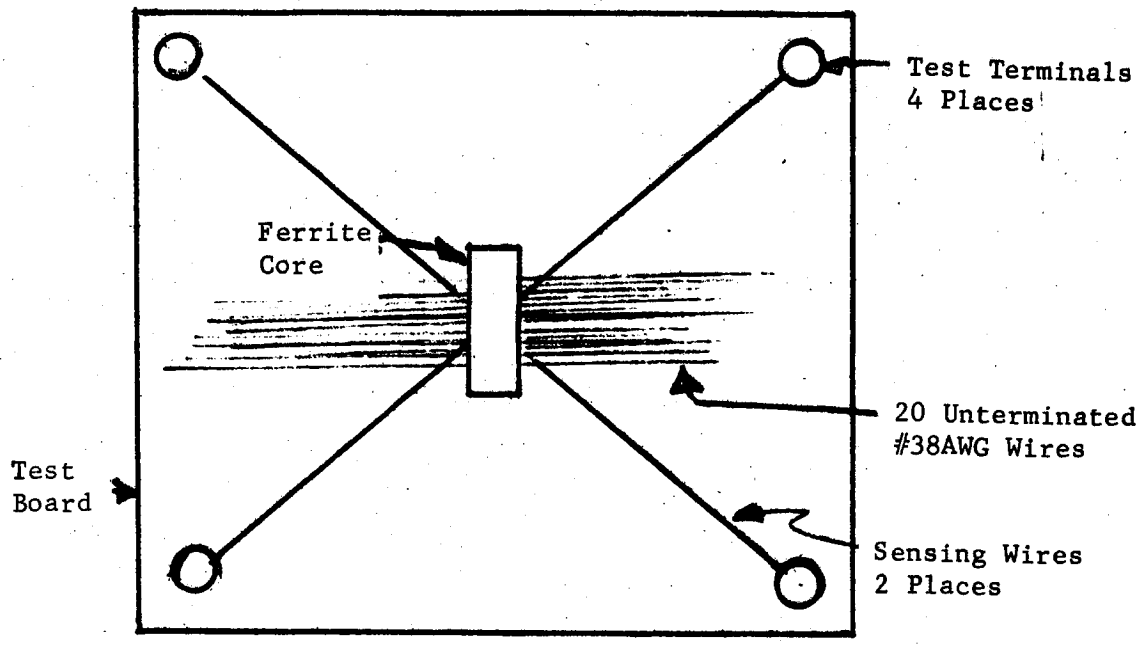


FIGURE H.5 EMBEDMENT STRESS TEST SPECIMEN CONFIGURATION

5. INSULATION REMOVAL TEST

5.1 Purpose - To determine the optimum method of removal of insulation from magnet wire. Heat, mechanical and chemical stripping methods are to be used.

5.2 Procedure

Note: After insulation is removed by any of the methods outlined below, the bare conductors are to be soldered into printed circuit board terminals and the solder joints examined for proper abhesion and fillet formation to insure complete insulation and contaminant removal.

5.2.1 Heat removal

1) Using a resistance wire loop (thermal stripper), heat insulated wire until insulation ignites or is loosened.

2) Remove insulation residue by wiping with a clean cloth.

5.2.2 Mechanical Removal

1) Remove insulation by abrading with a fine grit (No. 400) emery paper.

2) Remove residue by wiping with a clean cloth.

5.2.3 Chemical Removal

1) Immerse wire end into stripping solution until insulation is loosened.

2) Remove loosened insulation by wiping with a clean absorbent tissue.

3) Neutralize residual acids in a 5 percent sodium bicarbonate solution.

4) Wipe conductors dry with clean absorbent tissue.

5.3 Materials

1) No. 38 AWG copper magnet wire
2) Insulations: Polythermaleze (PTE), Heavy Formvar (HF), ML Polymer, and Solvar
3) No. 400 emery paper
4) Chemical Strippers: Strip-X, Strip-var, Lonco No. 3111, Lonco No. 416, HNO_3 (concentrated), HNO_3 (60 percent by volume).

6. WIRE STRENGTH TEST

6.1 Purpose - The purpose of this test is to determine the ultimate breaking strength of film insulated copper magnet wire.

6.2 Procedure

6.2.1 Single Wire

1) Insert test specimen into pull tester
2) Exert a steady continuous pull on the wire at at rate of 12 inches per minute
3) Record breaking force.

Note: Avoid kinking or sharp bends of the test wire. Any wire damaged by the jaws of the test apparatus shall be discarded. Wire breakage occurring because of wire kinking shall be disregarded as an invalid test specimen.

6.2.2 Double Wire

1) Insert two test wires through a ferrite cure
2) Insert ends of wires into pull tester
3) Record breaking force.

Note: The note of Procedure 1 applies. Additionally, evidence of cracking of the core will invalidate a particular test. Use a new core and new pair of wires for each test.

6.3 Materials and Equipment

1) Wire Terminal Pull Tester - Hunter Model TT-50
2) Mechanical Force Gage - Hunter Model D-50-1
3) No. 38 and No. 36 AWG Heavy Formvar insulated copper magnet wire
4) Lockheed Electronics 80-04 ferrite cores.

7. CORE SIRENGTH TEST

7.1 Purpose - The purpose of this test is to determine the breaking strength (tensile) of ferrite cores.

7.2 Procedure

7.2.1 Using two lengths of No. 36 AWG wire, install ferrite core into pull tester.

7.2.2 Exert continuous pull on the core at a rate of 12 feet per minute.

7.2.3 Record breaking force for the core.

Note: Disregard readings where the wire breaks. If a significant number of wire breaks occur, change the wire lot or use the next size larger wire.

7.3 Materials and Equipment

1) No. 36 AWG copper magnet wire
2) Lockheed Electronics 80-04 ferrite cores
3) Wire Terminal Pull Tester - Hunter Model TT-50
4) Mechanical Force Gage - Hunter Model D-50-1

APPENDIX I

TEST RESULTS AND DATA TABLES

1. Scrape Resistance
2. Abrasion Resistance
3. Cut Through Resistance

4a. Embedment Stress Analysis
b. Embedment Stress Data

5. Insulation Removal
6. Wire Strength
7. Core Strength

TABLE I.1 SCRAPE RESISTANCE TEST DATA
(Cycles to Failure)

	Sample Number																												
INSULATION TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Heavy Formvar	24	16	84	12	10	11	13	6	20	25	2	4	8	12	7	70	24	17	25	20	16	13	34	12	10	62	50	16	13	66
Heavy Polythermaleze	12	3	3	5	3	5	3	3	3	4	5	3	3	3	3	4	3	3	2	3	3	4	2	3	3	3	4	4	3	2
Heavy ML	3	3	3	4	3	3	4	7	7	6	4	4	4	3	5	5	8	2	7	4	7	4	7	6	4	4	3	5	3	4

	Range	Mean
HF	6 - 84	24
HP	2 - 12	4
HML	3 - 7	5

TABLE 1.2 ABRASION RESISTANCE

AMPEX CORE #480-67

5 Gms Wt									20 Gms Wt								
Sample No.	1	2	3	4	5	6	7	Mean	Sample No.	1	2	3	4	5	6	7	Mean
Insulation	Cycles to Failure								Insulation	Cycles to Failure							
Heavy Formvar	42	36	16	59	27	14	25	31	Heavy Formvar	24	19	13	10	9			15
Heavy Polythermaleze	30	51	40	100+	100+	53		62+	Heavy Polythermaleze	15	29	47	65	61			43
Heavy ML	100+	94	100+	100+	100+			99+	Heavy ML	43	60	90	81	77			71

AMPEX CORE #802-40

Sample No.	1	2	3	4	5	6	7	Mean	Sample No.	1	2	3	4	5	6	7	Mean
Insulation	Cycles to Failure								Insulation	Cycles to Failure							
Heavy Formvar	18	21	40	39	44	32		32	Heavy Formvar	15	17	19	13	17			16
Heavy Polythermaleze	78	100+	100+	100+	100+			36+	Heavy Polythermaleze	38	33	45	12	46	45		37
Heavy ML	100+	100+	100+	100+	100+			100+	Heavy ML	71	99	75	58	54			71

ELECTRONIC MEMORIES CORE #81-101A

Sample No.	1	2	3	4	5	6	7	Mean	Sample No.	1	2	3	4	5	6	7	Mean
Insulation	Cycles to Failure								Insulation	Cycles to Failure							
Heavy Formvar	27	30	18	18	18	23	29	23	Heavy Formvar	14	19	15	14	12			15
Heavy Polythermaleze	100+	99	100+	100+	100+			100+	Heavy Polythermaleze	32	38	35(1)	83(1)	42(1)			46+
Heavy ML	100+	100+	100+	100+	100+	100+		100+	Heavy ML	100+	100+	19(1)	29(1)	40(1)	50(1)		56+

ELECTRONIC MEMORIES CORE #81-104

Sample No.	1	2	3	4	5	6	7	Mean	Sample No.	1	2	3	4	5	6	7	Mean
Insulation	Cycles to Failure								Insulation	Cycles to Failure							
Heavy Formvar	42	48	17	33	37	30		35	Heavy Formvar	21	13	17	15	16			16
Heavy Polythermaleze	100+	60	95	100+	77	100+		89+	Heavy Polythermaleze	40(1)	44(1)	52(1)	55	51			48+
Heavy ML	100+	100+	100+	100+	100+			100+	Heavy ML	100(1)	100(1)	34(1)	90(1)	100(1)			85+

LOCKHEED CORE #80-04

Sample No.	1	2	3	4	5	6	7	Mean	Sample No.	1	2	3	4	5	6	7	Mean
Insulation	Cycles to Failure								Insulation	Cycles to Failure							
Heavy Formvar	49	35	47	51	35			43	Heavy Formvar	20	19	19	23	26			21
Heavy Polythermaleze	99	100+	100+	100+	100+			100+	Heavy Polythermaleze	55(1)	25(1)	50(1)	34(1)	39			41
Heavy ML	69	100+	100+	100+	100+			94+	Heavy ML	97(1)	100+	85(1)	96(1)	100+			96+

(1) Number of cycles run at 20 gms on those which did not fail @ 5 gms.

TABLE I.3 CUT THROUGH RESISTANCE TEST

Wire Insulation	Core Condition	No. Pass (Each Sample Size-50)	No. Fail	% Passed
Formvar	Coated (Krylon)	33	17	66
Formvar	Uncoated	19	31	38
Solvar	Coated (Krylon)	16	34	32
Solvar	Uncoated	8	42	16

Average improvement of coated over uncoated cures - 87%

TABLE I.4a EMBEDMENT STRESS ANALYSIS

Cure Schedule Temperature	80° C
Thermal Sterilization Temperature	145° C
Normal Operating Temperature	-10° C to 85° C
Dimension of Ferrite Core	O.D. = .080 inch
	I.D. = .050 inch
	Thickness = .025 inch

Thermal Expansion Coefficients:

Ferrite	$X_1 = 27 \times 10^{-6}$ in/ in/°C
Silicon Rubber	$X_2 = 110 \times 10^{-6}$ in/ in/°C
Epoxy	$X_3 = 23 \times 10^{-6}$ in/ in/°C

Relationship $S = \epsilon E$

$$\epsilon = \frac{\Delta 1}{1}$$

Where: E = Young's Modules

ϵ = Strain

S = Stress

1 = in/in/°C

$\Delta 1$ = change in/in/°C

I. STRESS imposed when ring is cooled to 25° C from 80° C

80° C - 25° C = 55° C

$$\epsilon 1 = \frac{1}{1} = - \frac{(27 - 23) \times 10^{-6} \times (55° C) xt}{1} = -4 \times 10^{-6} \times (+58)$$

$$= +2.2 \times 10^{-4}$$

$$S = \mp 2.2 \times 10^{-6} \times 29^{E} \times 10^{6} \times 10^{2} = -63.8 \times 10^{2}$$

$$= 6,380 \text{ psi}$$

Tensil and Shear

Above case when adhesion is present, when adhesion is not present shrinkage of ring in embedment takes place.

II. Stress imposed when ring is cycled to 145° C

$145° - 80°C = 65° C$

$$\epsilon_2 = 4 \times 10^{-6} \times 65° = 260 \times 10^{-6} = 2.6 \times 10^{-4}$$

$$S = \epsilon E = 2.6 \times 10^{-4} \times 29 \times 10^{6} = 75.4 \times 10^{2}$$

$$= 7,540 \text{ psi compressive stress}$$

III. Stress imposed on rign when ring is cycled to -10° C

$80° - (-10C) = 90° C$

$$\epsilon = 4.6 \times 10^{-6} \times 90 = 4.14 \times 10^{-4}$$

$$S = 4.14 \times 10^{-x} \times 29 \times 10^{6}$$

$$= 120 \times 10^{2} = 12,000 \text{ psi}$$

IV. Stress imposed on ring when conformally coated (3 mils) with silicone rubber, embedded and temperature cycled to 145° C

Rubber to Ferrite

$$\epsilon_1 = (110 - 27) \times 10^{-6} \times 65 = 5,395 \times 10^{-6}$$

$$= 5.4 \times 10^{-3}$$

$$S_1 = 5.4 \times 10^{-3} \times 1 \times 10^{4} = 54 \text{ psi}$$

Rubber to Epoxy

$$\epsilon_2 = (110 - 23) \times 10^{-6} \times 65 = 5655 \times 10^{-6}$$

$$= 5.7 \times 10^{-3}$$

$$S_1 = 5.7 \times 10^{-3} \times 1 \times 10^{4} = 57 \text{ psi}$$

Combined Stress is 54 + 57 = 111 psi

V. Stress imposed on ri when conformally coated (3 mils) with silicon rubber, embedded and temperature cycled to -10° C

$$80 - (-10) = 90$$

Rubber to Ferrite

$$\epsilon_3 = (10 - 27) \times 10^{-6} \times 90 = 7.5 \times 10^{-3}$$

$$S_3 = 75 \times 10^{-3} \times 1 \times 10^{4} = 75 \text{ psi tensile}$$

Rubber to Epoxy

$$\epsilon_4 = (110 - 23) \times 10^{-6} \times 90 = 7.93 \times 10^{-3}$$

$$S_4 = 7.93 \times 10^{-3} \times 1 \times 10^{4} = 79 \text{ psi tensile}$$

Combined tensile stress is 79 + 75 = 154 psi.

TABLE I.4b EMBEDMENT STRESS DATA

		uV_1 (mv)		T_D (μsec)		T_P (μsec)		T_{TS} (μsec)		T_S (μsec)	
Core	No	Unpotted	Potted	Unpotted	Potted	Unpotted	Potted	Unpotted	Potted	Unpotted	Potted
A	7	176.0	48.0	0.36	0.04	1.01	0.76	1.52	1.52	1.16	1.48
A	8	178.0	33.0	0.35	0.04	1.01	0.76	1.52	1.54	1.17	1.50
A	12	174.0	47.5	0.35	0.04	1.01	0.81	1.53	1.54	1.18	1.50
A	19	175.2	38.0	6.38	0.04	1.01	0.81	1.53	1.56	1.15	1.52
A	20	172.0	39.0	0.36	0.03	1.01	0.66	1.53	1.34	1.17	1.31
A	21	175.2	43.0	0.33	0.04	1.00	0.80	1.53	1.53	1.20	1.49
A	23	182.0	57.5	0.37	0.05	1.00	0.81	1.48	1.53	1.11	1.48
A	24	184.8	31.0	0.38	0.12	1.00	0.76	1.48	1.56	1.10	1.44
A	25	185.0	32.0	0.40	0.12	1.00	0.72	1.48	1.56	1.08	1.44
A	26	186.0	47.0	0.37	0.04	1.00	0.78	1.50	1.53	1.13	1.49
B	1	173.0	176.0	0.36	0.35	1.01	1.00	1.51	1.48	1.15	1.13
B	3	179.6	180.0	0.39	0.34	1.01	1.01	1.50	1.49	1.11	1.15
B	5	175.0	176.8	0.32	0.34	1.01	1.00	1.50	1.48	1.18	1.15
B	6	176.3	179.0	0.31	0.32	1.01	1.01	1.50	1.47	1.19	1.15
B	10	175.0	180.5	0.35	0.36	1.01	1.00	1.53	1.48	1.18	1.12
B	15	173.5	179.2	0.35	0.32	1.01	1.01	1.53	1.48	1.18	1.16
B	16	174.0	179.8	0.37	0.32	1.02	1.00	1.53	1.45	1.16	1.13
B	22	173.0	178.0	0.36	0.34	1.01	1.00	1.53	1.49	1.17	1.15
B	28	178.0	175.0	0.38	0.34	1.02	1.01	1.50	1.50	1.12	1.16
C	2	178.0	179.0	0.39	0.33	1.01	1.00	1.50	1.45	1.11	1.12
C	4	179.5	180.8	0.29	0.32	1.01	1.00	1.50	1.46	1.21	1.14
C	9	141.5	175.4	0.37	0.32	1.02	1.00	1.53	1.46	1.16	1.14
C	11	176.2	180.0	0.38	0.32	1.01	1.00	1.53	1.46	1.15	1.14
C	13	170.5	175.5	0.33	0.30	1.01	0.99	1.52	1.46	1.19	1.16
C	14	172.0	16.9	0.38		1.02		1.53		1.15	
C	17	174.0	180.0	0.37	0.28	1.01	0.98	1.52	1.42	1.15	1.14
C	18	173.2	180.0	0.37	0.30	1.02	1.00	1.53	1.46	1.16	1.16
C	27	178.0	127.5	0.36	0.36	1.01	1.00	1.51	1.47	1.15	1.11

A = Epoxy Potting
B = RTV11 with Epoxy Overcoat
C = Sylgard 182 with Epoxy Overcoat

TABLE I.5 INSULATION REMOVAL

Insulation Stripper or Method	Wire Type	Immersion Time	Post Treatment	Observation
1. Heat	PTE	-	-	Oxides formed on conductor surface. Amount of heat must be carefully controlled. Yield and tensile values are reduced approx. 60%, but are 80-90% restored after oxides are removed by abraision.
	HF	-	-	
	ML	-	-	
2. Mechanical Strip	PTE	-	-	Hand abraded with abrasive paper. Yield and tensile are not appreciably altered.
	HF	-	-	
	ML	-	-	
3. Strip-X	PTE	2 min.	None	Removal satisfactory.
	HF	1.5"	None	Removal satisfactory.
	ML	3."	None	No effect.
4. Strip-var	PTE	2 min	None	Removal - Satisfactory
	HF	1.5"	None	Removal - Satisfactory
	ML	3 "	None	No effect.
5. Lonco 3111	HPT	3/4-1-1/2 min	$Na\ Hco_3$	Complete removal conductor bright & shiny.
	HF	3/4-1-1/2 "	$Na\ Hco_3$	Complete removal conductor bright & shiny.
	ML	3/4-1-1/2 "	$Na\ Hco_3$	No effect.
6. Lonco #416	HPT	1-1/2-2 min.	$Na\ Hco_3$	Complete removal conductor bright & shiny.
	HF	1-1/2-2 "	$Na\ Hco_3$	Complete removal conductor bright & shiny.
	ML	3 "	$Na\ Hco_3$	No effect.
7. HNO_3 (conc)	HPT	3-7 sec.	$N2Hco_3$	Complete removal conductor bright
	HF	3-7 "	$N2Hco_3$	Complete removal conductor bright
	ML	1 min	$N2Hco_3$	No effect.
8. HNO_3 60% HNO_3 by vol.	HPT	1/2-3/4 min	$NaHco_3$	Complete removal conductor bright
	HF	1/2-3/4	$NaHco_3$	Complete removal conductor bright
	ML	3 min.	$NaHco_3$	No effect.

TABLE I.6 WIRE STRENGTH

Procedure 1 (Single #36 AWG Heavy Formvar Wire between jaws)

Sample No.	Breaking Force (lbs)	Sample No.	Breaking Force (lbs)
1	0.80	11	0.75
2	0.75	12	0.90
3	0.90	13	0.90
4	0.80	14	0.80
5	0.75	15	0.90
6	0.90	16	0.75
7	0.95	17	0.90
8	0.80	18	0.90
9	0.80	19	0.80
10	0.85	20	0.75

Range - 0.75 to 0.95
Mean - 0.83

Procedure 2 (Two wires inserted in ferrite core)

A. #38 AWG HF (Anaconda)

Sample No.	Breaking Force (lbs)	Sample No.	Breaking Force (lbs)
1	1.5	11	1.3
2	1.2	12	1.4
3	1.1	13	1.2
4	1.2	14	1.2
5	1.2	15	1.4
6	1.2	16	1.2
7	1.4	17	1.1
8	1.1	18	1.3
9	1.4	19	1.1
10	1.2	20	1.5

Range - 1.1 to 1.5
Mean - 1.3

TABLE I.6 (Continued)

B. #38 AWG HF (Essex)

Sample No.	Breaking Force (lbs)	Sample No.	Breaking Force (lbs)
1	0.7	11	0.8
2	0.8	12	0.7
3	1.2	13	0.9
4	0.8	14	1.0
5	0.7	15	1.0
6	0.9	16	0.8
7	0.8	17	0.9
8	0.8	18	1.1
9	0.7	19	0.8
10	1.1	20	0.9

Range - 0.7 to 1.2
Mean - 0.9

C. #36 AWG HF (Anaconda)

Sample No.	Breaking Force (lbs)	Sample No.	Breaking Force (lbs)
1	1.6	11	1.7
2	1.6	12	1.6
3	1.2	13	1.7
4	1.8	14	1.8
5	1.7	15	1.2
6	1.1	16	1.5
7	1.8	17	1.3
8	1.7	18	1.7
9	1.8	19	1.2
10	1.5	20	1.3

Range - 1.1 to 1.8
Mean - 1.5

TABLE I.7 CORE STRENGTH

Ampex Core 48067 - #36 AWG Heavy Formvar (wire doubled)

Sample No.	Breaking Force (lbs)	Sample No.	Breaking Force (lbs)
1	2.6	11	2.6
2	2.6	12	2.6
3	2.4	13	2.6
4	2.6	14	2.5
5	2.3	15	2.6
6	2.5	16	0.9*
7	2.4	17	2.5
8	2.5	18	2.4
9	2.7	19	2.6
10	2.4	20	2.6

*This sample disregarded.

Range - 2.3 to 2.7
Mean - 2.5